

Project Name :PF4PN2F
Platform : AMD Picasso+N17S-G2

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30. POWER_1.0VA/+1.8VA
31. POWER +1.2VS/2.5VS/VTT
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41. N17S-G2 VRAM2_FrameBuffer A
42. N17S-G2 NVVDD
43. N17S-G2 1V8_AON/1V8_MAIN/PEX
44. N17S-G2 FBVDDQ_MEM
45. Other/SCREW
46. HISTORY

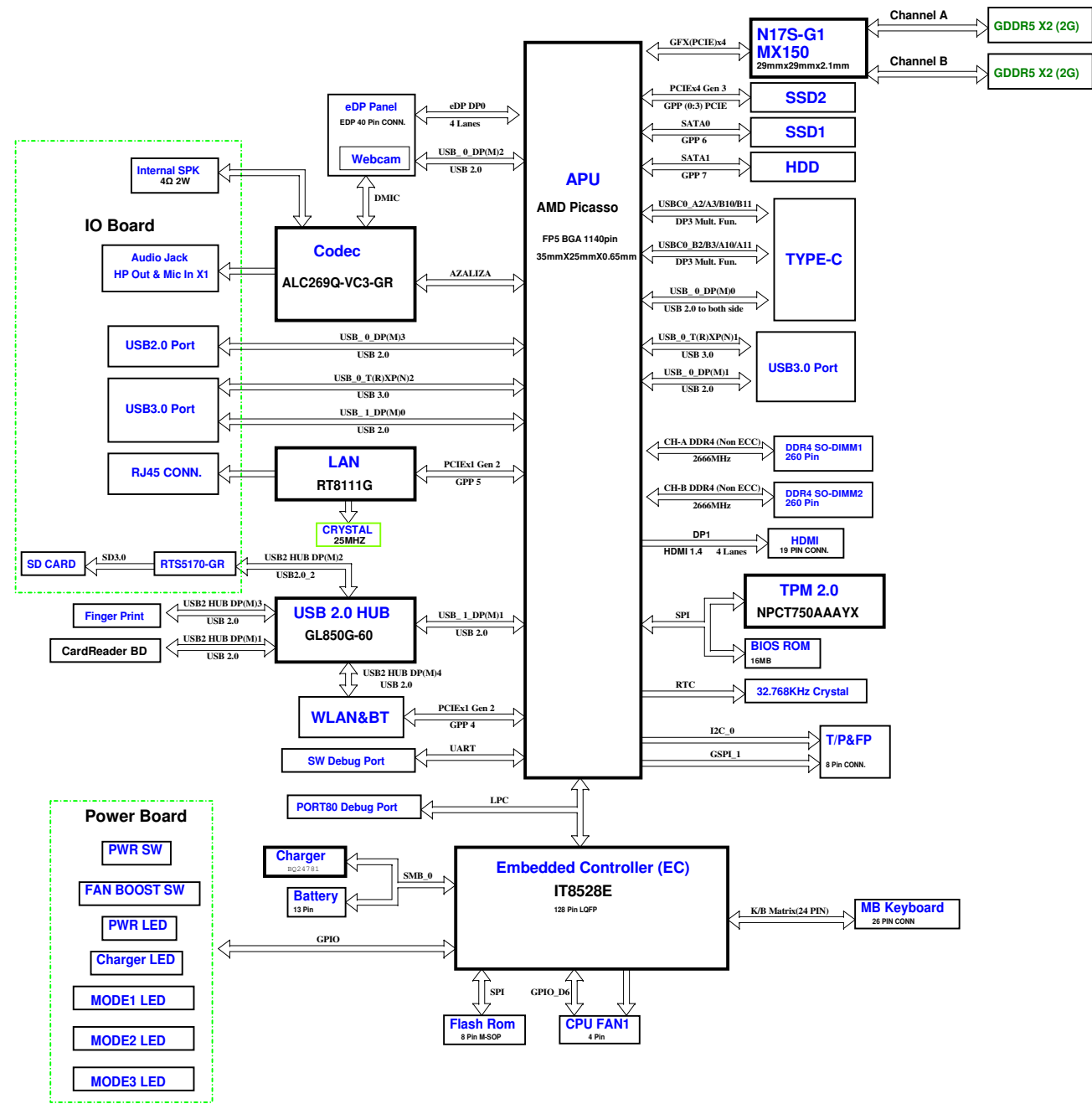
M/B Schematic Version Change List

[illegible]

Daughter Board Schematic Version Change List

[illegible]

SYSTEM BLOCK DIAGRAM





MA_DM[0:7] >>MA_DM[0:7] 11
MA_MA[0:13] >>MA_MA[0:13] 11
MA_MD[0:63] <<>MA_MD[0:63] 11
MA_DQS[0:7] <<>MA_DQS[0:7] 11
MA_DQS#[0:7] <<>MA_DQS#[0:7] 11

MEMORY A

MA_MA0 AF25
MA_WA1 AE23
MA_MA3 AD29
MA_MA3 AE21
MA_MA4 AC24
MA_MA5 AC26
MA_MA5 AD21
MA_MA7 AC27
MA_MA5 AD22
MA_MA9 AC21
MA_MA10 AF22
MA_MA11 AA24
MA_MA12 AC23
MA_MA13 AJ25
MA_WE# <<< AG27
MA_CAS# <<< AG23
MA_RAS# <<< AG26
MA_BA0 <<< AF21
MA_BA1 <<< AF27
MA_BG0 <<< AA21
MA_BG1 <<< AA27
MA_ACT# <<< AA22
MA_DM0 F21
MA_DM1 G27
MA_DM2 N24
MA_DM3 N23
MA_DM4 AL24
MA_DM5 AW27
MA_DM6 AW25
MA_DM7 AT21
MA_DQS0 F22
MA_DQS#0 G22
MA_DQS1 H27
MA_DQS#1 H26
MA_DQS2 N27
MA_DQS#2 N26
MA_DQS3 P21
MA_DQS#3 P21
MA_DQS4 AM26
MA_DQS#4 AM27
MA_DQS5 AN24
MA_DQS#5 AN25
MA_DQS6 AU23
MA_DQS#6 AT23
MA_DQS7 AV20
MA_DQS#7 AW20
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MA_CLK#0 <<< AD24
MA_CLK1 <<< AE26
MA_CLK#1 <<< AE27
MA_CS#0 <<< AG21
MA_CS#1 <<< AJ27
MA_CKE0 <<< Y23
MA_CKE1 <<< Y26
MA_ODT0 <<< AG24
MA_ODT1 <<< AJ22
MA_ALERT# <<< AA25
MA_EVENT# <<< AE24
MA_RESET# <<< Y24

MA_ADD0/RSVD
MA_ADD1/RSVD
MA_ADD2/MAB_CA5
MA_ADD3/RSVD
MA_ADD4/RSVD
MA_DATA0/MAB_CA0
MA_ADD6/MAB_CA2
MA_ADD7/MAB_CA4
MA_ADD8/MAB_CA3
MA_ADD9/MAB_CA1
MA_ADD10/RSVD
MA_ADD11/RSVD
MA_ADD12/RSVD
MA_ADD13_BANK2/MAB_CA0
MA_WE_L_ADD14/MAB_CA2
MA_CAS_L_ADD15/MAB_CA1
MA_RAS_L_ADD16/MAB_CA3
MA_BANK0/MAB_CA4
MA_BANK1/RSVD
MA_BG0/MAB_CA5
MA_BG1/RSVD
MA_ACT_L/RSVD
MA_DM0/MAB_DM1
MA_DM1/MAB_DM0
MA_DM2/MAB_DM2
MA_DATA26/MAB_DATA26
MA_DM4/MAB_DM2
MA_DM5/MAB_DM3
MA_DM6/MAB_DM1
MA_DM7/MAB_DM0
RSVD_36
MA_DQS_H0/MAB_DQS_H1
MA_DQS_L0/MAB_DQS_L1
MA_DQS_H1/MAB_DQS_H0
MA_DQS_L1/MAB_DQS_L0
MA_DQS_H2/MAB_DQS_H2
MA_DQS_L2/MAB_DQS_L2
MA_DQS_H3/MAB_DQS_H3
MA_DQS_L3/MAB_DQS_L3
MA_DQS_H4/MAB_DQS_H4
MA_DQS_L4/MAB_DQS_L4
MA_DQS_H5/MAB_DQS_H5
MA_DQS_L5/MAB_DQS_L5
MA_DQS_H6/MAB_DQS_H6
MA_DQS_L6/MAB_DQS_L6
MA_DQS_H7/MAB_DQS_H7
MA_DQS_L7/MAB_DQS_L7
RSVD_41
RSVD_40
MA_CLK_H0/MAB_CK1
MA_CLK_L0/MAB_CK0
MA_CLK_H1/MAB_CK1
MA_CLK_L1/MAB_CK0
MA_CS_L0/MAB_CS1
MA_CS_L1/MAB_CS0
MA_CKE0/MAB_CKE0
MA_CKE1/MAB_CKE1
MA_ODT0/RSVD
MA_ODT1/RSVD
MA_ALERT_L/MAB_TEST
MA_EVENT_L
MA_RESET_L

MA_DATA0/MAB_DATA0
MA_DATA1/MAB_DATA0
MA_DATA2/MAB_DATA1
MA_DATA3/MAB_DATA1
MA_DATA4/MAB_DATA1
MA_DATA5/MAB_DATA1
MA_DATA6/MAB_DATA1
MA_DATA7/MAB_DATA1
MA_DATA8/MAB_DATA7
MA_DATA9/MAB_DATA1
MA_DATA10/MAB_DATA5
MA_DATA11/MAB_DATA4
MA_DATA12/MAB_DATA0
MA_DATA13/MAB_DATA6
MA_DATA14/MAB_DATA2
MA_DATA15/MAB_DATA3
MA_DATA16/MAB_DATA17
MA_DATA17/MAB_DATA16
MA_DATA18/MAB_DATA3
MA_DATA19/MAB_DATA2
MA_DATA20/MAB_DATA19
MA_DATA21/MAB_DATA18
MA_DATA22/MAB_DATA21
MA_DATA23/MAB_DATA22
MA_DATA24/MAB_DATA30
MA_DATA25/MAB_DATA31
MA_DATA26/MAB_DATA26
MA_DATA27/MAB_DATA27
MA_DATA28/MAB_DATA28
MA_DATA29/MAB_DATA29
MA_DATA30/MAB_DATA24
MA_DATA31/MAB_DATA25
MA_DATA32/MAB_DATA16
MA_DATA33/MAB_DATA17
MA_DATA34/MAB_DATA22
MA_DATA35/MAB_DATA20
MA_DATA36/MAB_DATA19
MA_DATA37/MAB_DATA18
MA_DATA38/MAB_DATA23
MA_DATA39/MAB_DATA21
MA_DATA40/MAB_DATA30
MA_DATA41/MAB_DATA31
MA_DATA42/MAB_DATA26
MA_DATA43/MAB_DATA27
MA_DATA44/MAB_DATA28
MA_DATA45/MAB_DATA29
MA_DATA46/MAB_DATA24
MA_DATA47/MAB_DATA25
MA_DATA48/MAB_DATA11
MA_DATA49/MAB_DATA10
MA_DATA50/MAB_DATA15
MA_DATA51/MAB_DATA13
MA_DATA52/MAB_DATA13
MA_DATA53/MAB_DATA13
MA_DATA54/MAB_DATA9
MA_DATA55/MAB_DATA8
MA_DATA56/MAB_DATA6
MA_DATA57/MAB_DATA7
MA_DATA58/MAB_DATA2
MA_DATA59/MAB_DATA3
MA_DATA60/MAB_DATA4
MA_DATA61/MAB_DATA5
MA_DATA62/MAB_DATA1
MA_DATA63/MAB_DATA0
RSVD_34
RSVD_35
RSVD_51
RSVD_52
RSVD_27
RSVD_28
RSVD_43
RSVD_42
MA_PAROUT/RSVD

FPS REV 1.11
PART 1 OF 13
FPS

MB_DM[0:7] >>MB_DM[0:7] 11
MB_MA[0:13] >>MB_MA[0:13] 12
MB_MD[0:63] <<>MB_MD[0:63] 12
MB_DQS[0:7] <<>MB_DQS[0:7] 12
MB_DQS#[0:7] <<>MB_DQS#[0:7] 12

MEMORY B

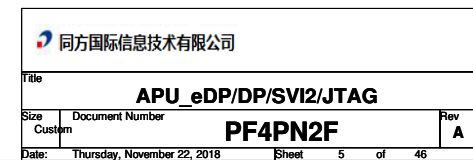
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MB_MA1 AC32
MB_MA2 AC30
MB_MA3 AB29
MB_MA4 AB31
MB_MA5 AA30
MB_MA6 AA29
MB_MA7 Y30
MB_MA8 AA31
MB_MA9 W29
MB_MA10 AH29
MB_MA11 Y32
MB_MA12 W31
MB_MA13 AL30
MB_WE# <<< AK30
MB_CAS# <<< AK32
MB_RAS# <<< AJ30
MB_BA0 <<< AH31
MB_BA1 <<< AG32
MB_BG0 <<< V31
MB_BG1 <<< V29
MB_ACT# <<< V30
MB_DM0 C21
MB_DM1 C25
MB_DM2 E32
MB_DM3 K30
MB_DM4 AP30
MB_DM5 AW31
MB_DM6 BB26
MB_DM7 BD22
MB_DQS0 D22
MB_DQS#0 B22
MB_DQS1 D25
MB_DQS#1 B25
MB_DQS2 F29
MB_DQS#2 F30
MB_DQS3 K31
MB_DQS#3 K29
MB_DQS4 AR29
MB_DQS#4 AR31
MB_DQS5 AW30
MB_DQS#5 AW29
MB_DQS6 BC25
MB_DQS#6 BA25
MB_DQS7 BC22
MB_DQS#7 BA22
MB_CS#0 <<< AC31
MB_CS#1 <<< AD30
MB_CLK0 <<< AD29
MB_CLK#0 <<< AD31
MB_CLK1 <<< AE30
MB_CLK#1 <<< AE32
MB_CS#0 <<< AF31
MB_CS#1 <<< AF31
MB_CKE0 <<< U29
MB_CKE1 <<< T30
MB_ODT0 <<< U31
MB_ODT1 <<< U31
MB_ALERT# <<< AL31
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MB_RESET# <<< AL29
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MB_EVENT# <<< AG29
MB_RESET# <<< T31

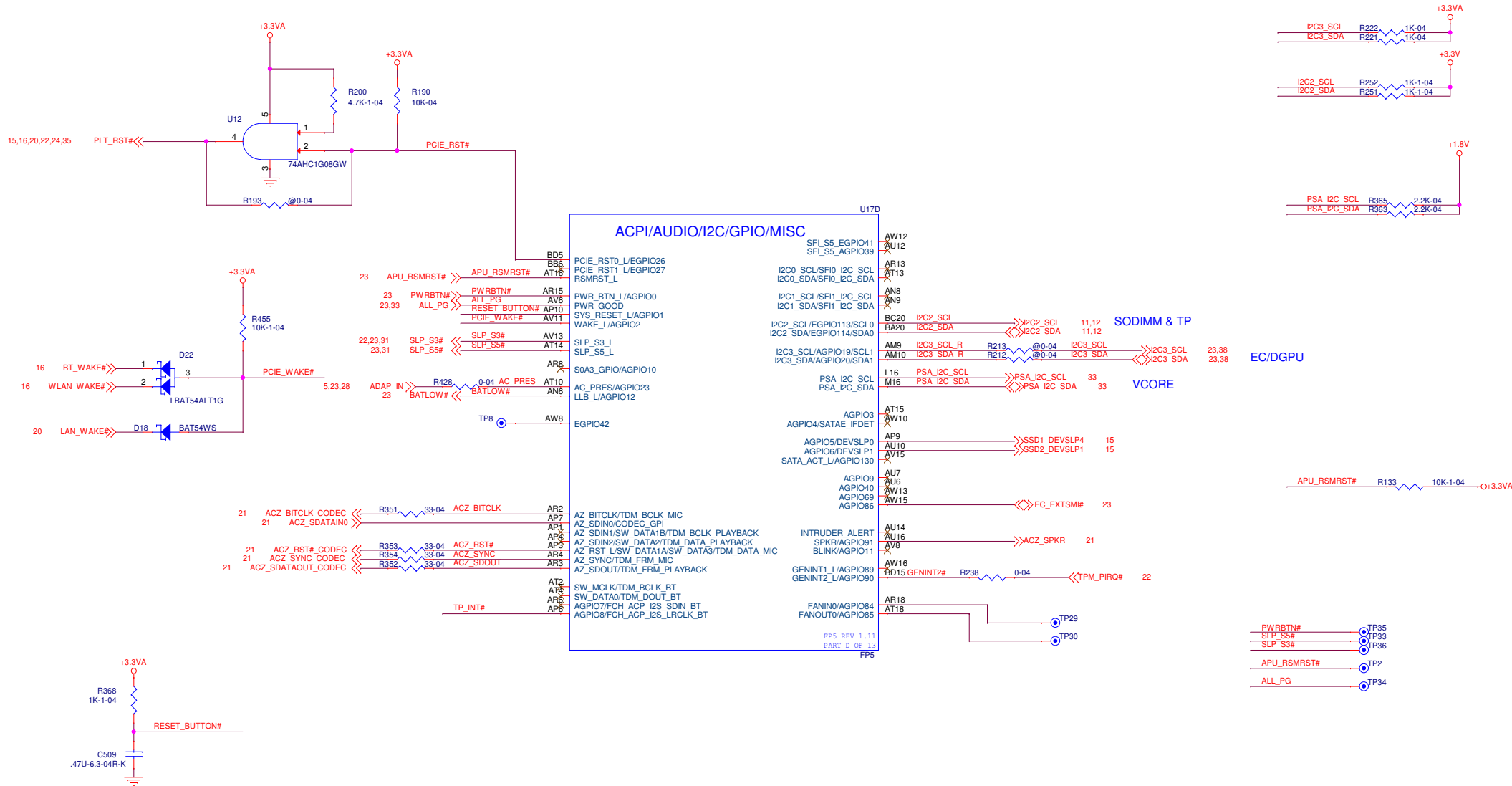
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MB_ADD2/MBB_CA5
MB_ADD3/RSVD
MB_ADD4/RSVD
MB_ADD5/MBA_CA0
MB_ADD6/MBA_CA2
MB_ADD7/MBA_CA2
MB_ADD8/MBA_CA3
MB_ADD9/MBA_CA1
MB_ADD10/RSVD
MB_ADD11/RSVD
MB_ADD12/RSVD
MB_ADD13_BANK2/MBB_CA0
MB_WE_L_ADD14/MBB_CA2
MB_CAS_L_ADD15/MBB_CA1
MB_RAS_L_ADD16/MBB_CA3
MB_BANK0/MBB_CA4
MB_BANK1/RSVD
MB_BG0/MBA_CA5
MB_BG1/RSVD
MB_ACT_L/RSVD
MB_DM0/MBA_DM1
MB_DM1/MBA_DM0
MB_DM2/MBA_DM2
MB_DM3/MBA_DM5
MB_DM4/MBB_DM2
MB_DM5/MBB_DM3
MB_DM6/MBB_DM1
MB_DM7/MBB_DM0
RSVD_21
MB_DQS_H0/MBA_DQS_H1
MB_DQS_L0/MBA_DQS_L1
MB_DQS_H1/MBA_DQS_H0
MB_DQS_L1/MBA_DQS_L0
MB_DQS_H2/MBA_DQS_H2
MB_DQS_L2/MBA_DQS_L2
MB_DQS_H3/MBA_DQS_H3
MB_DQS_L3/MBA_DQS_L3
MB_DQS_H4/MBB_DQS_H2
MB_DQS_L4/MBB_DQS_L2
MB_DQS_H5/MBB_DQS_H3
MB_DQS_L5/MBB_DQS_L3
MB_DQS_H6/MBB_DQS_H1
MB_DQS_L6/MBB_DQS_L1
MB_DQS_H7/MBB_DQS_H0
MB_DQS_L7/MBB_DQS_L0
RSVD_20
RSVD_18
MB_CLK_H0/MBA_CK1
MB_CLK_L0/MBA_CK0
MB_CLK_H1/MBB_CK1
MB_CLK_L1/MBB_CK0
RSVD/MBA_CS1
RSVD/MBA_CS0
RSVD/MBB_CKE0
RSVD/MBB_CKE1
MB0_CS_L0/MBB_CS1
MB0_CS_L1/MBB_CS0
RSVD_89
RSVD_90
MB0_CKE0/MBA_CKE0
MB0_CKE1/MBA_CKE1
RSVD/MAB_CS0
RSVD/MAB_CS1
MB0_ODT0/RSVD
MB0_ODT1/RSVD
RSVD/MAB_CKE0
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MB_ALERT_L/MAB_TEST
MB_EVENT_L
MB_RESET_L

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PART 1 OF 13
FPS

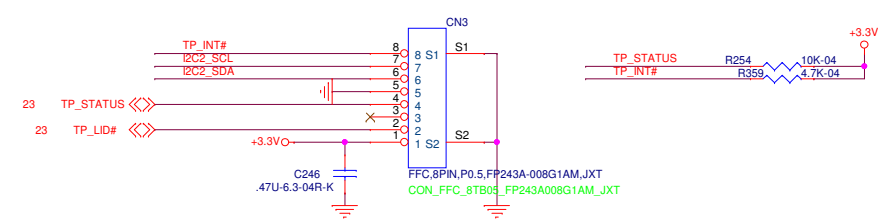
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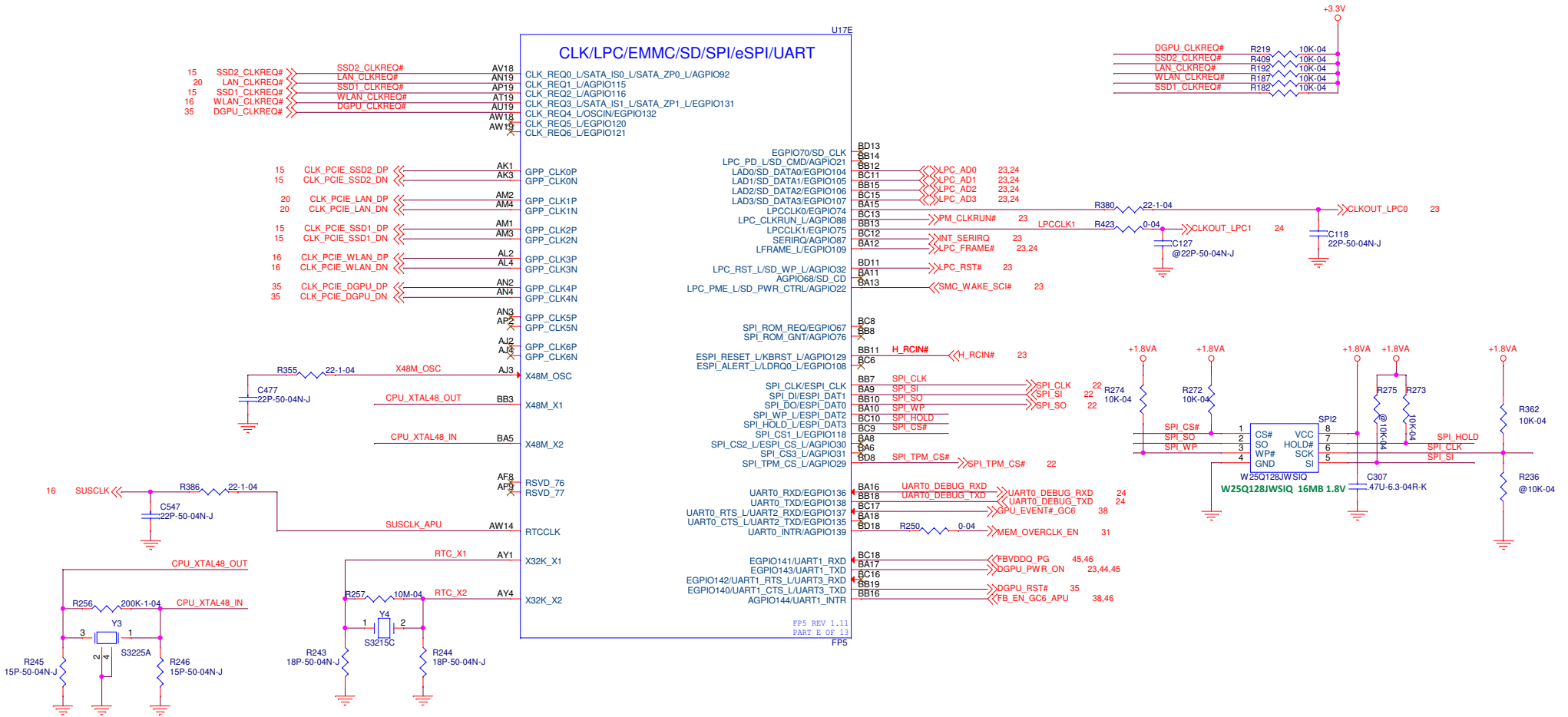


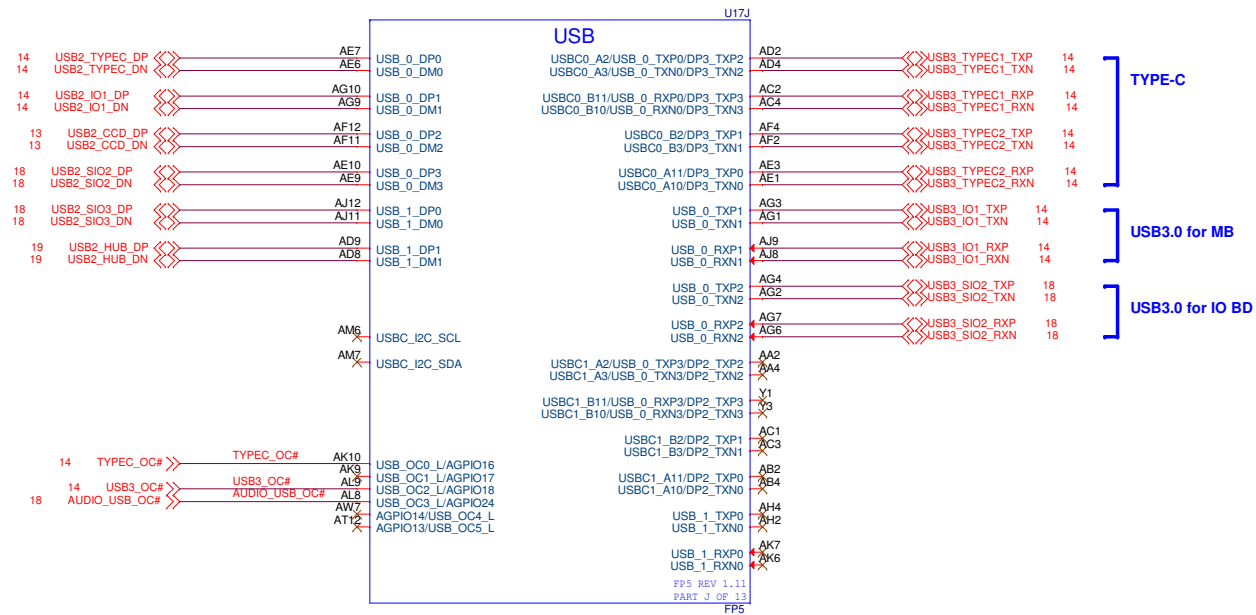


Touch Pad CONN

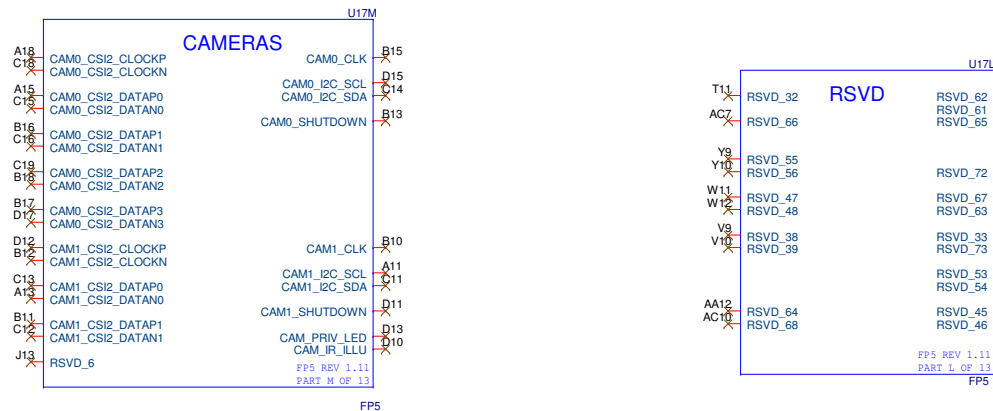


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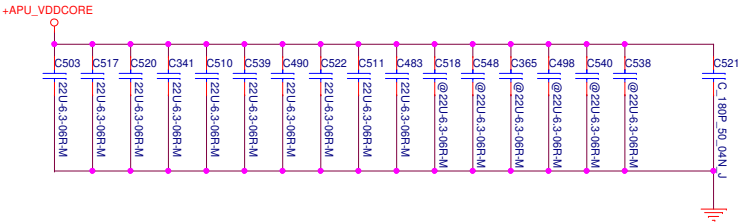




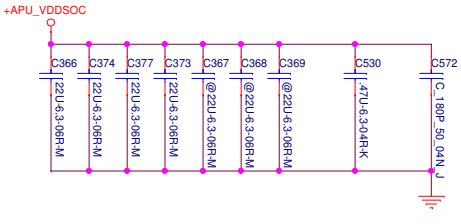
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USB_0_0	TYPE-C Port
USB_0_1	USB3.0 Port
USB_0_2	Web Camera
USB_0_3	USB2.0 PORT on IO DB
USB_1_0	USB3.0 Port on IO DB
USB_1_1	USB 2.0 HUB
HUB 0	USB 1_1
HUB 1	CarReader on CarReader DB
HUB 2	CardReader on IO DB
HUB 3	FINGER PRINTER
HUB 4	Bluetooth



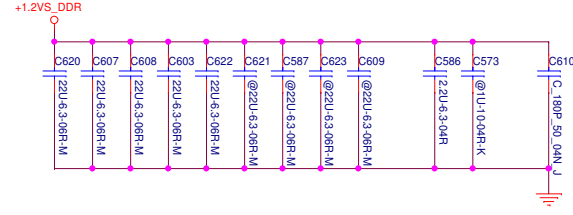
VDDCR
Under the APU



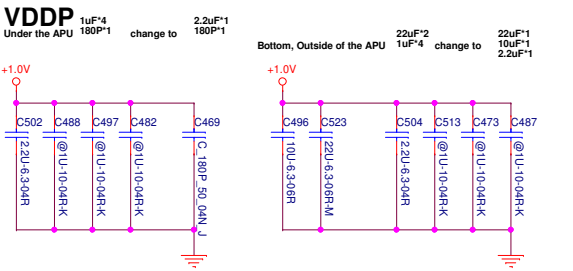
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Under the APU



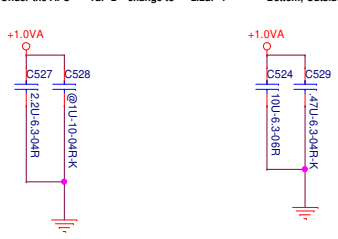
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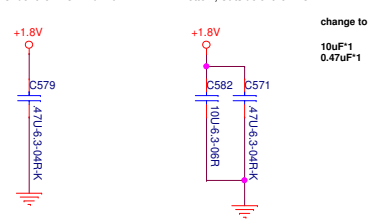
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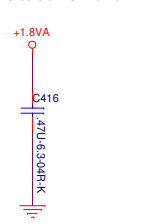
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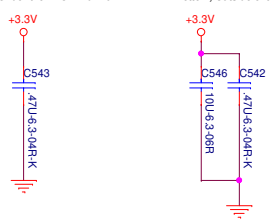
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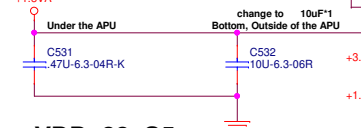
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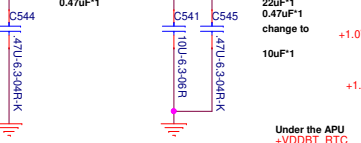
VDD_33



VDDIO_AUDIO



VDD_33_S5

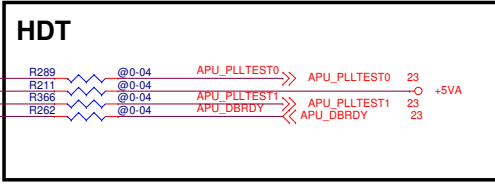
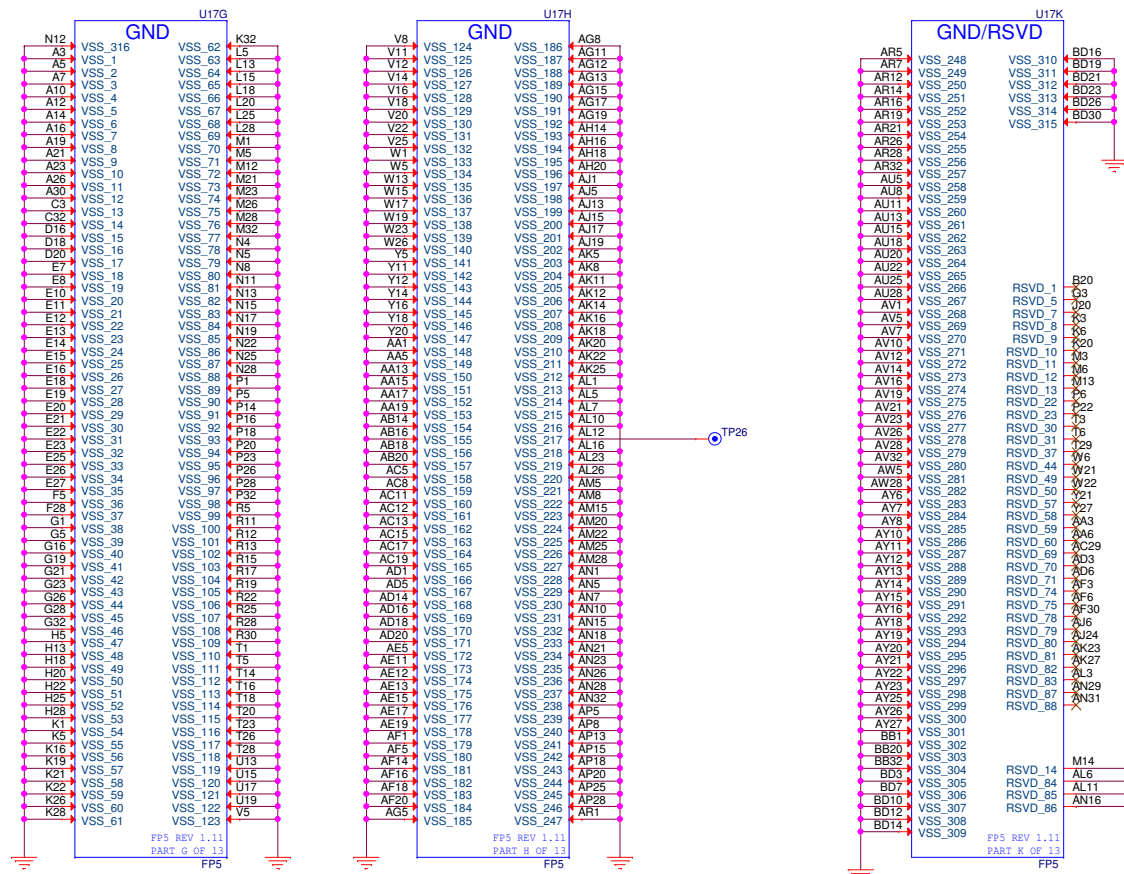


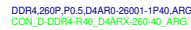
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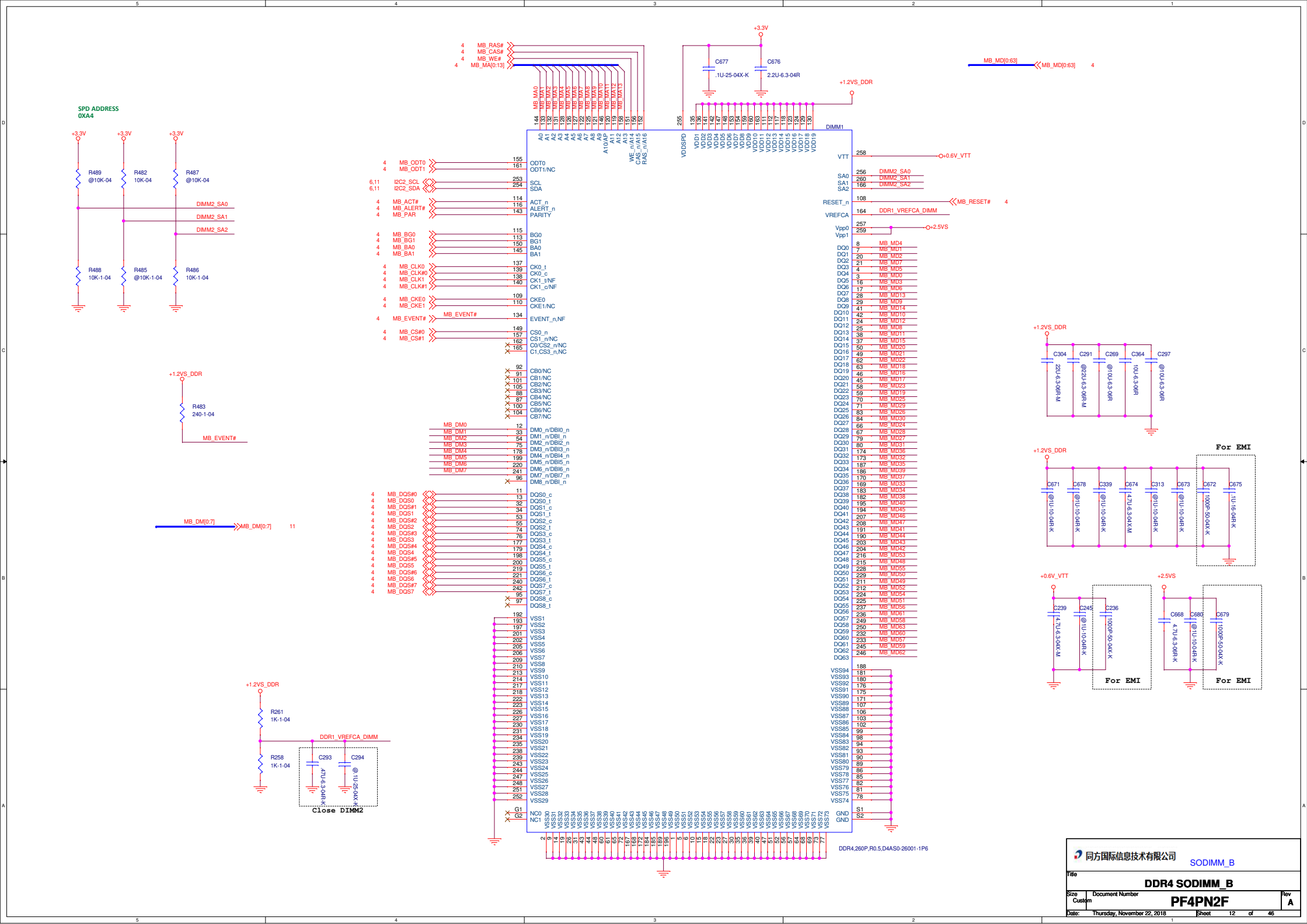


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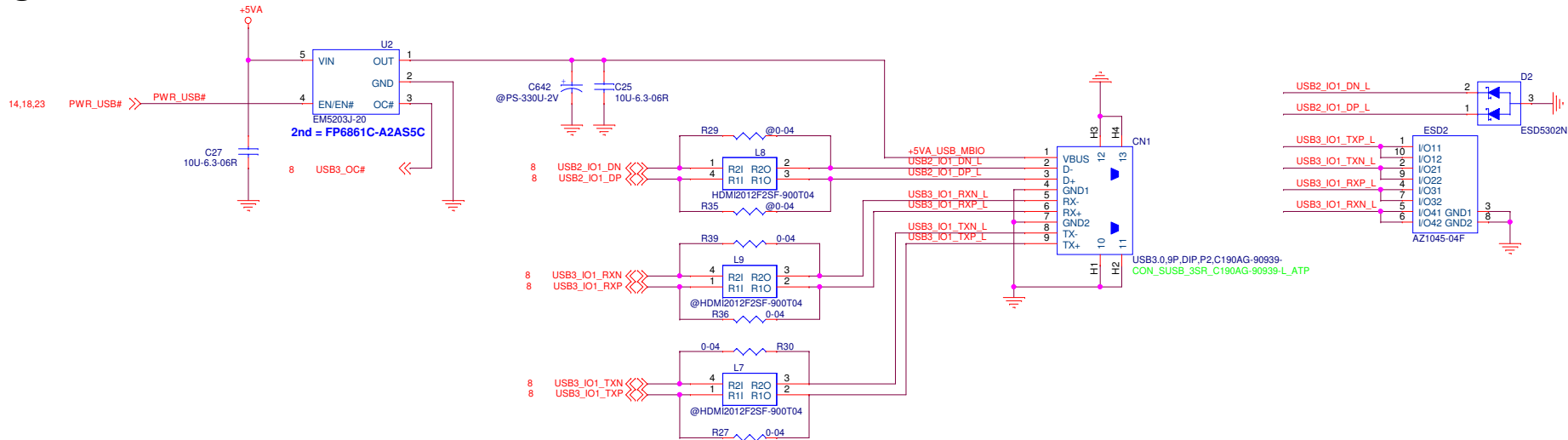
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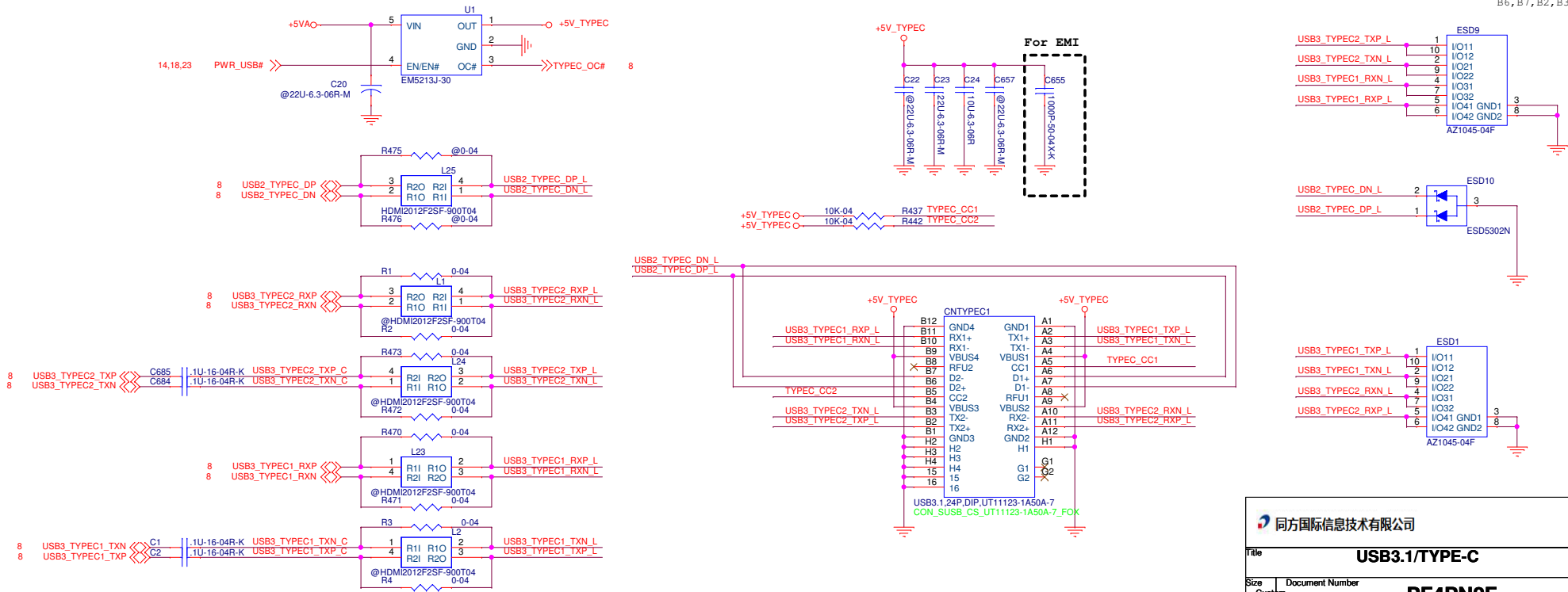




USB3.0 CONN.



USB3.0 TYPE-C

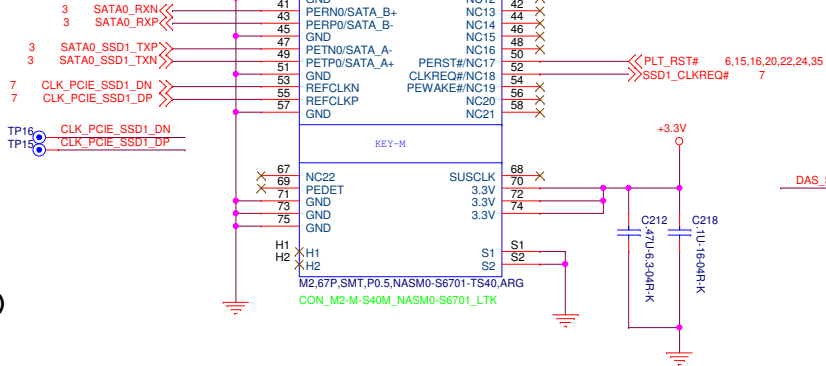


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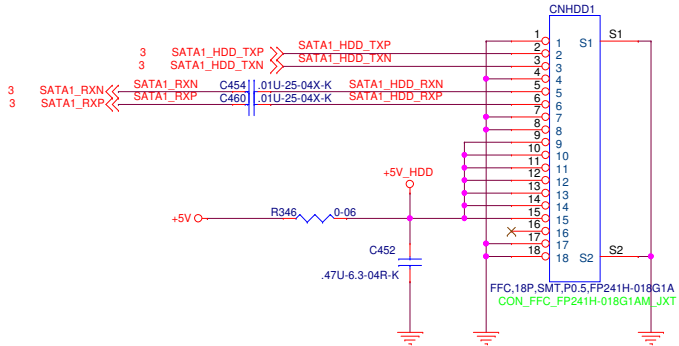
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HDD

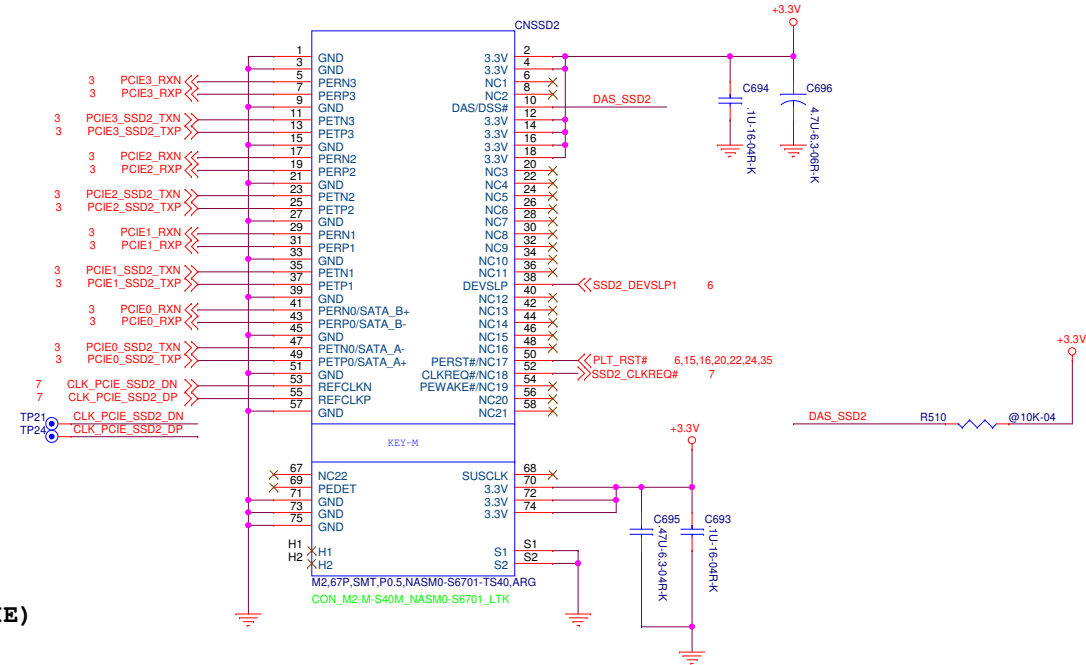
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(only SATA)



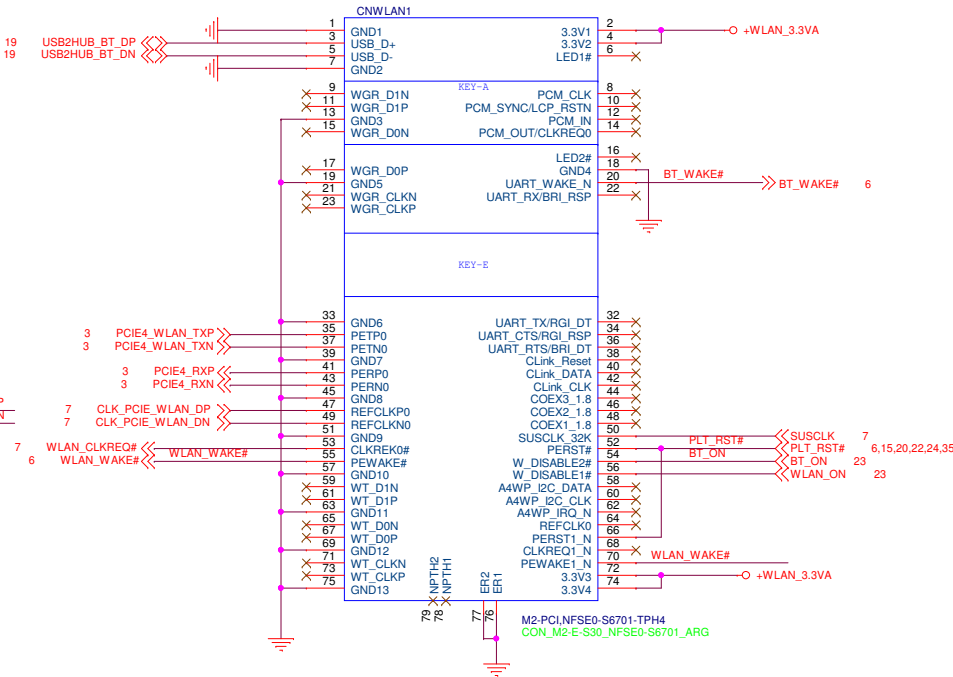
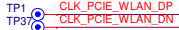
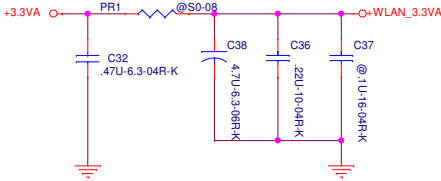
SSD2



(only PCIE)

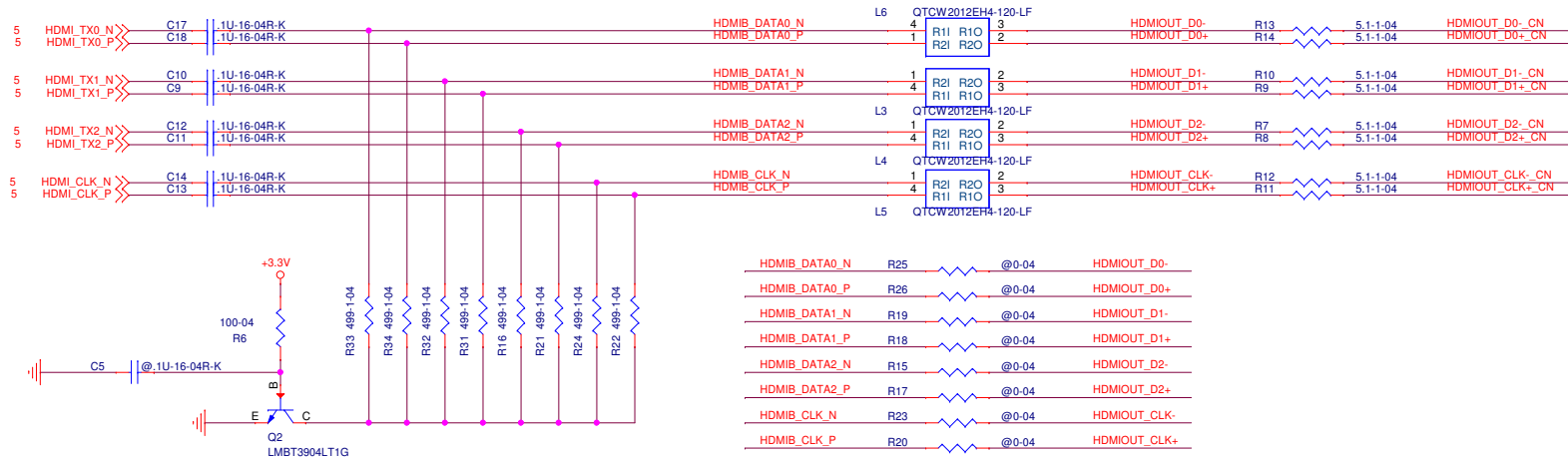
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WLAN CONN

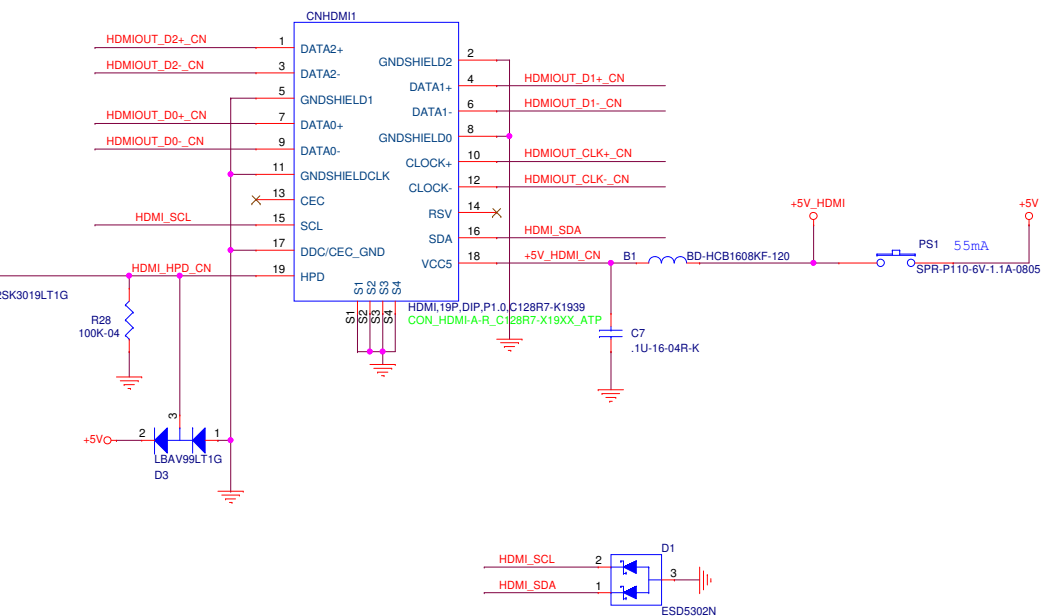


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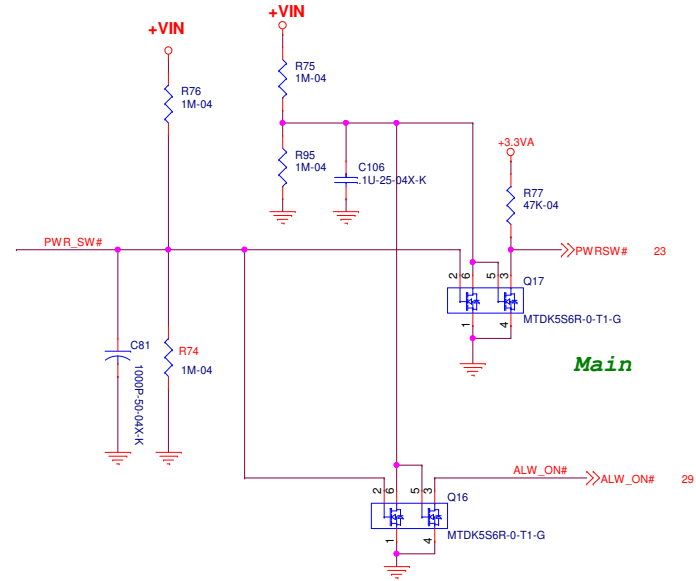
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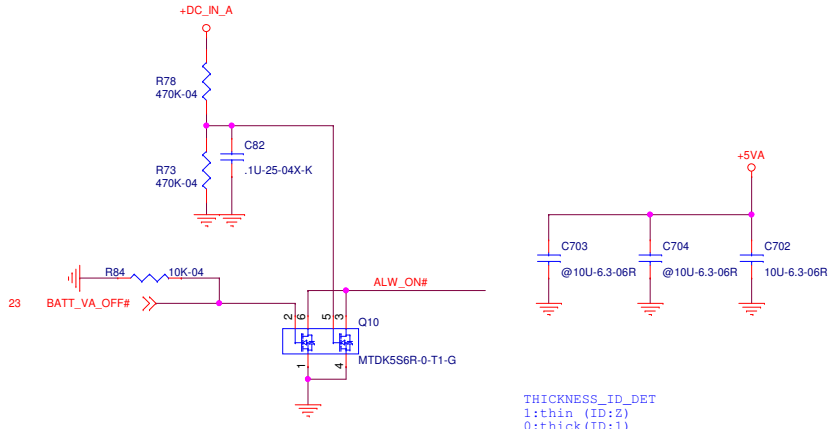
HDMI CONN



POWER SW

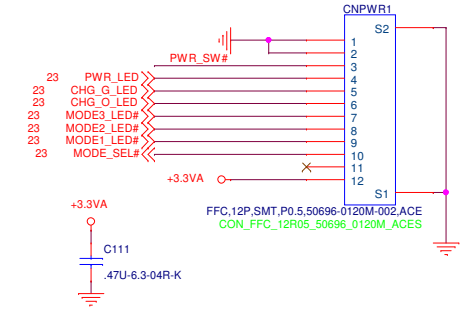


Main

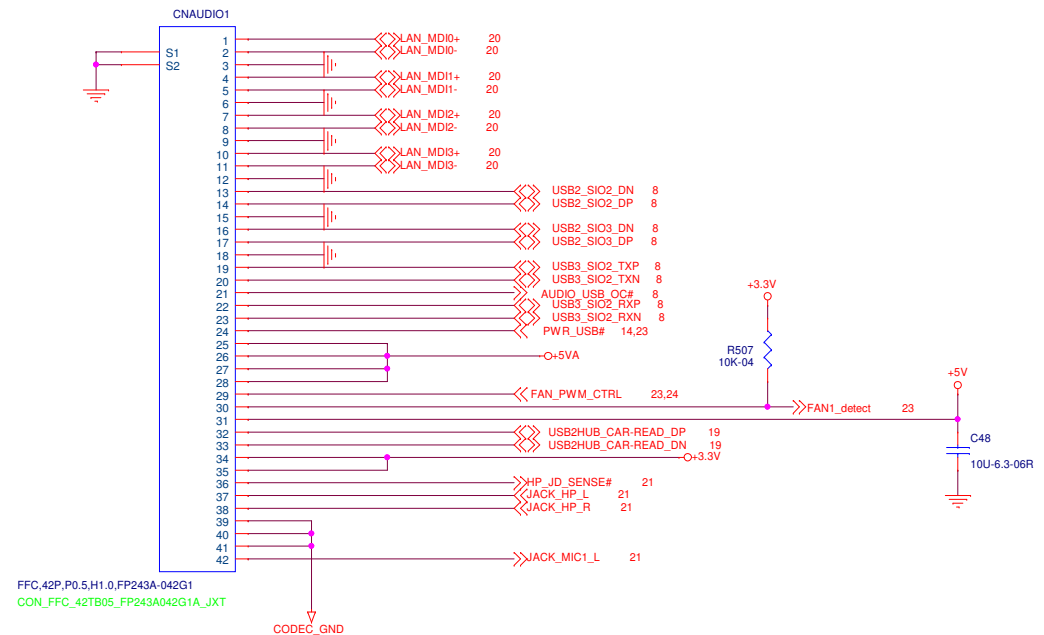


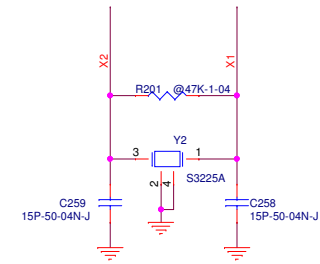
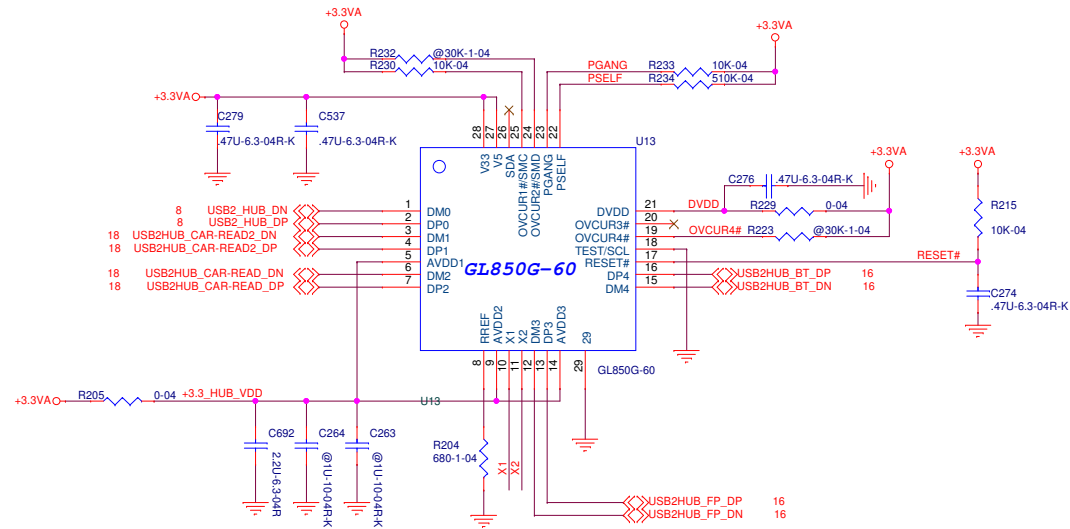
THICKNESS_ID_DET
1:thin (ID:2)
0:thick (ID:1)

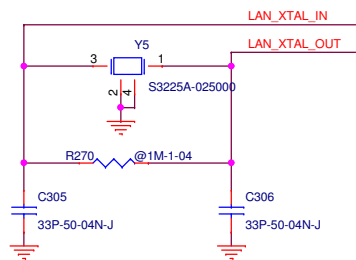
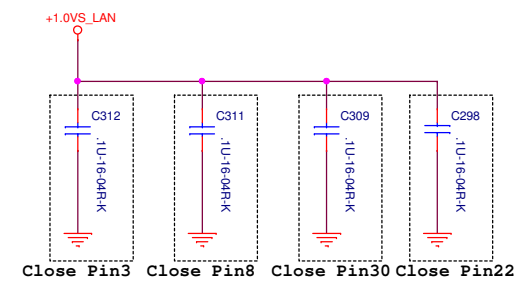
POWER DB CONN.

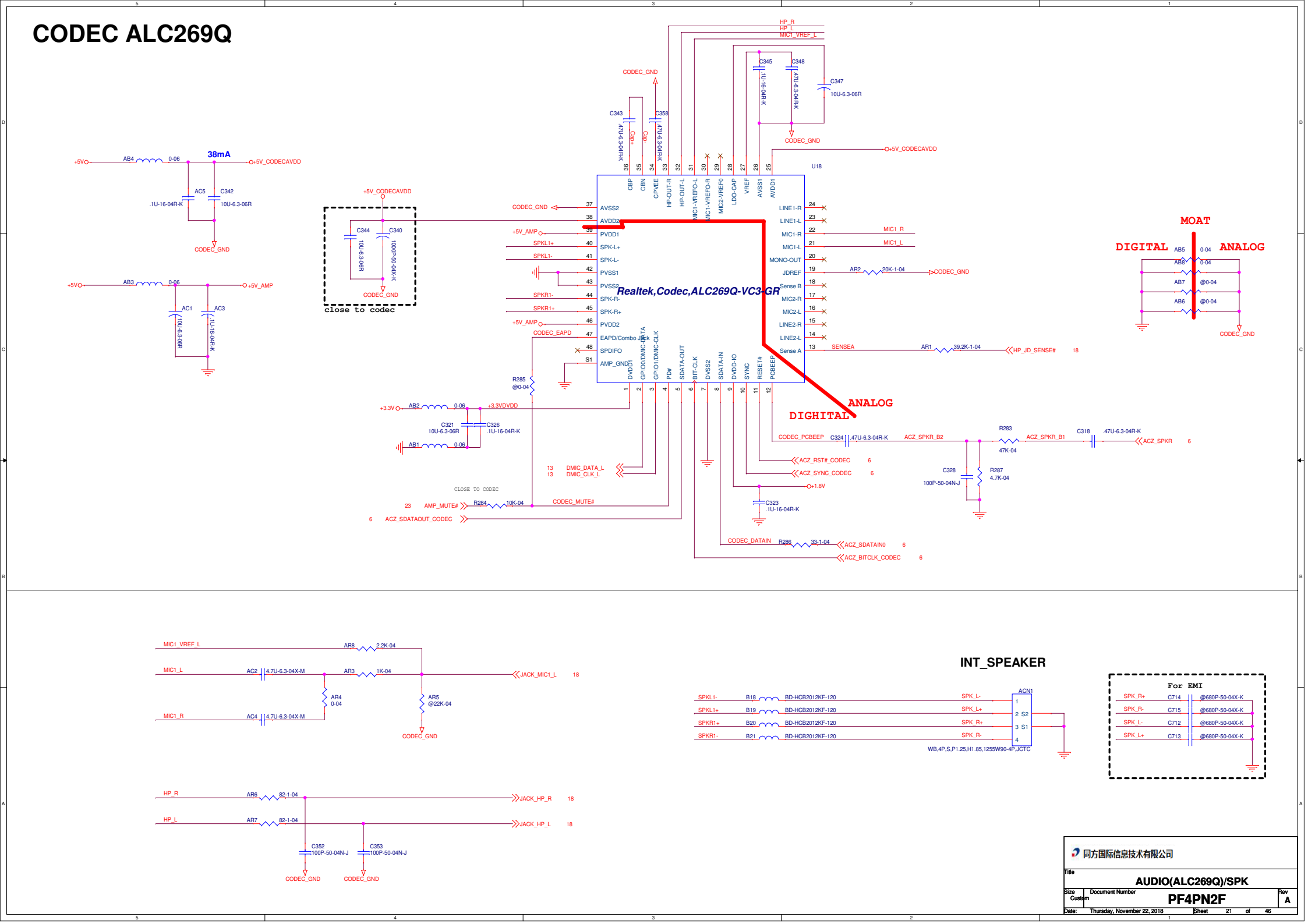
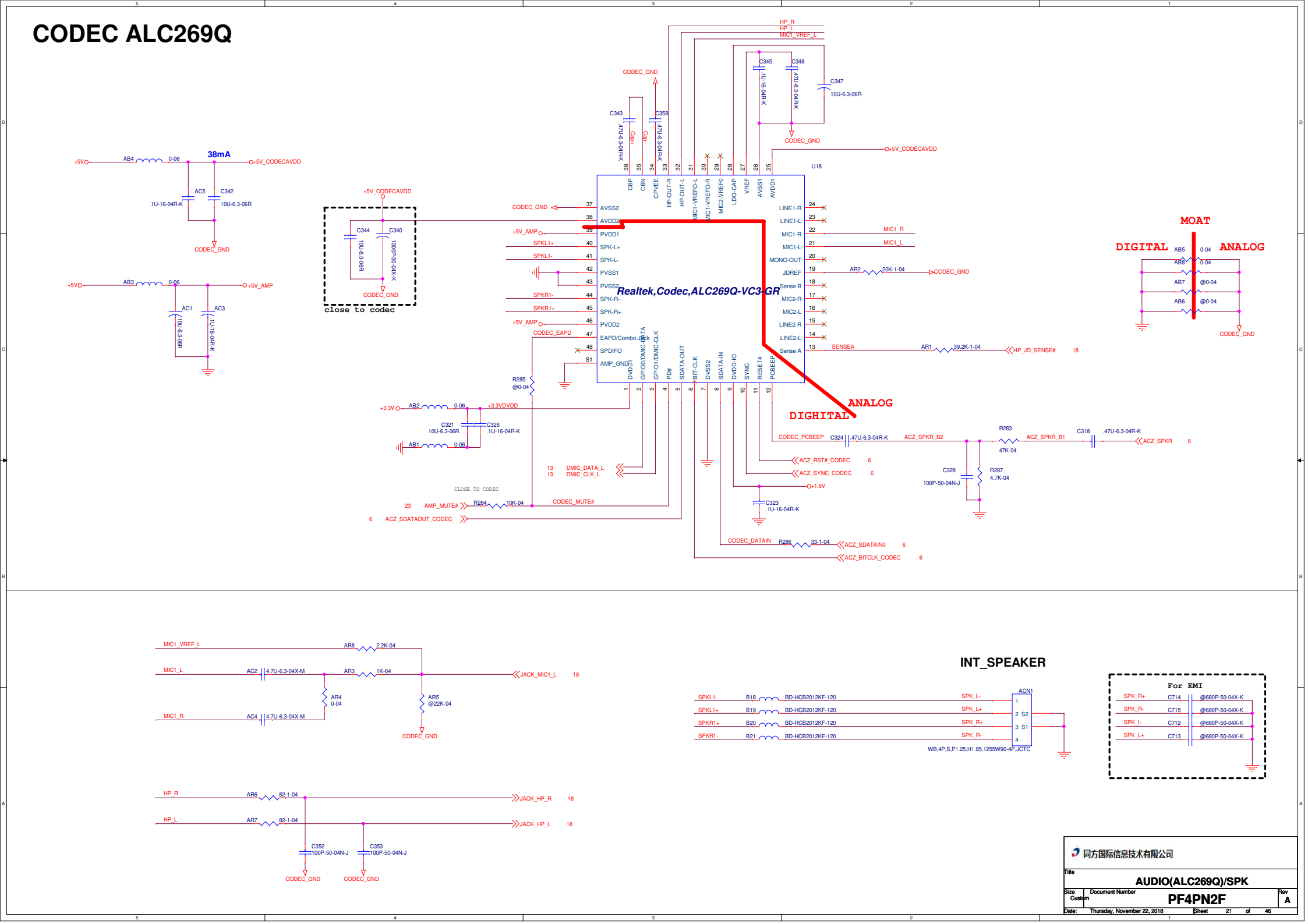
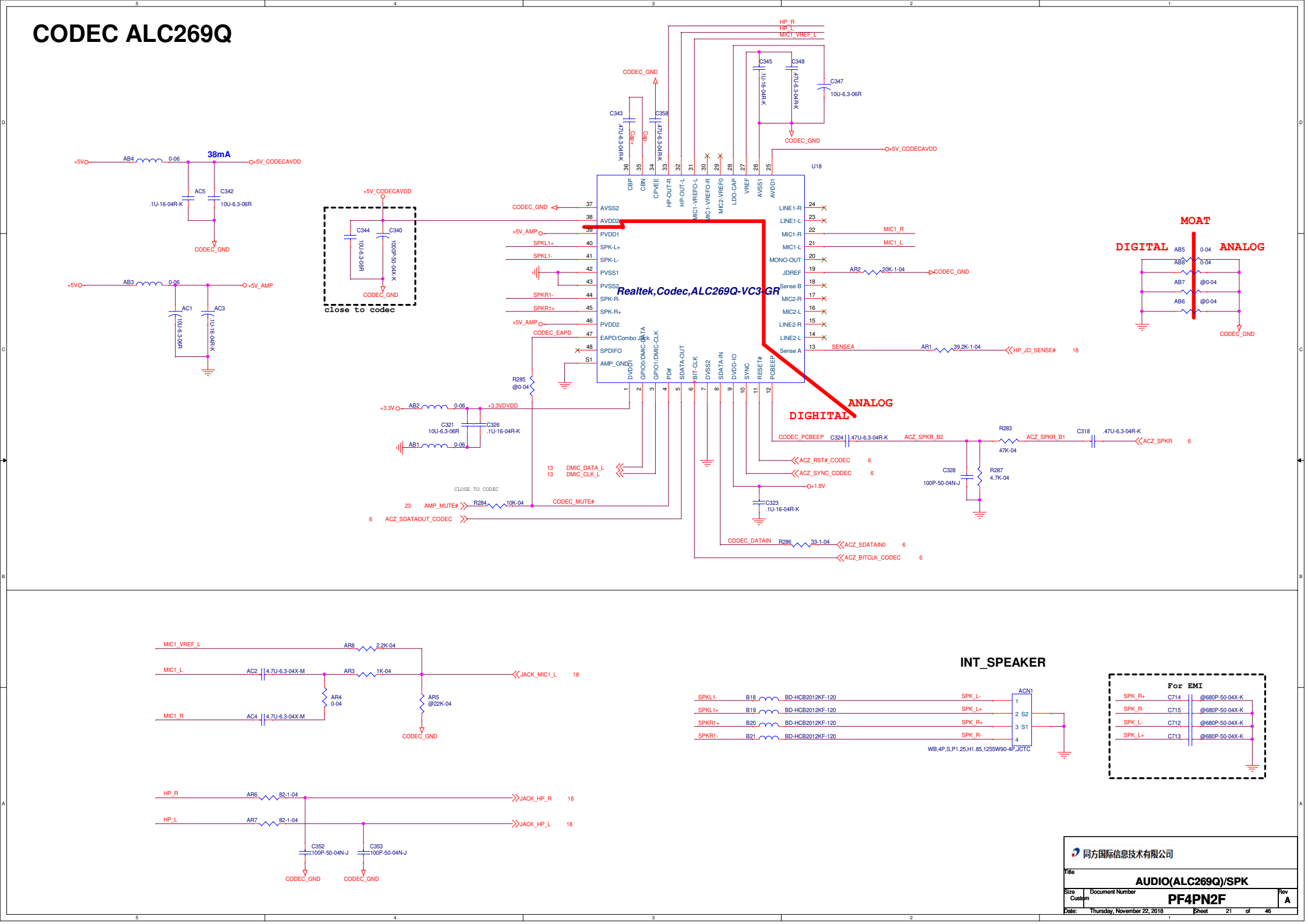


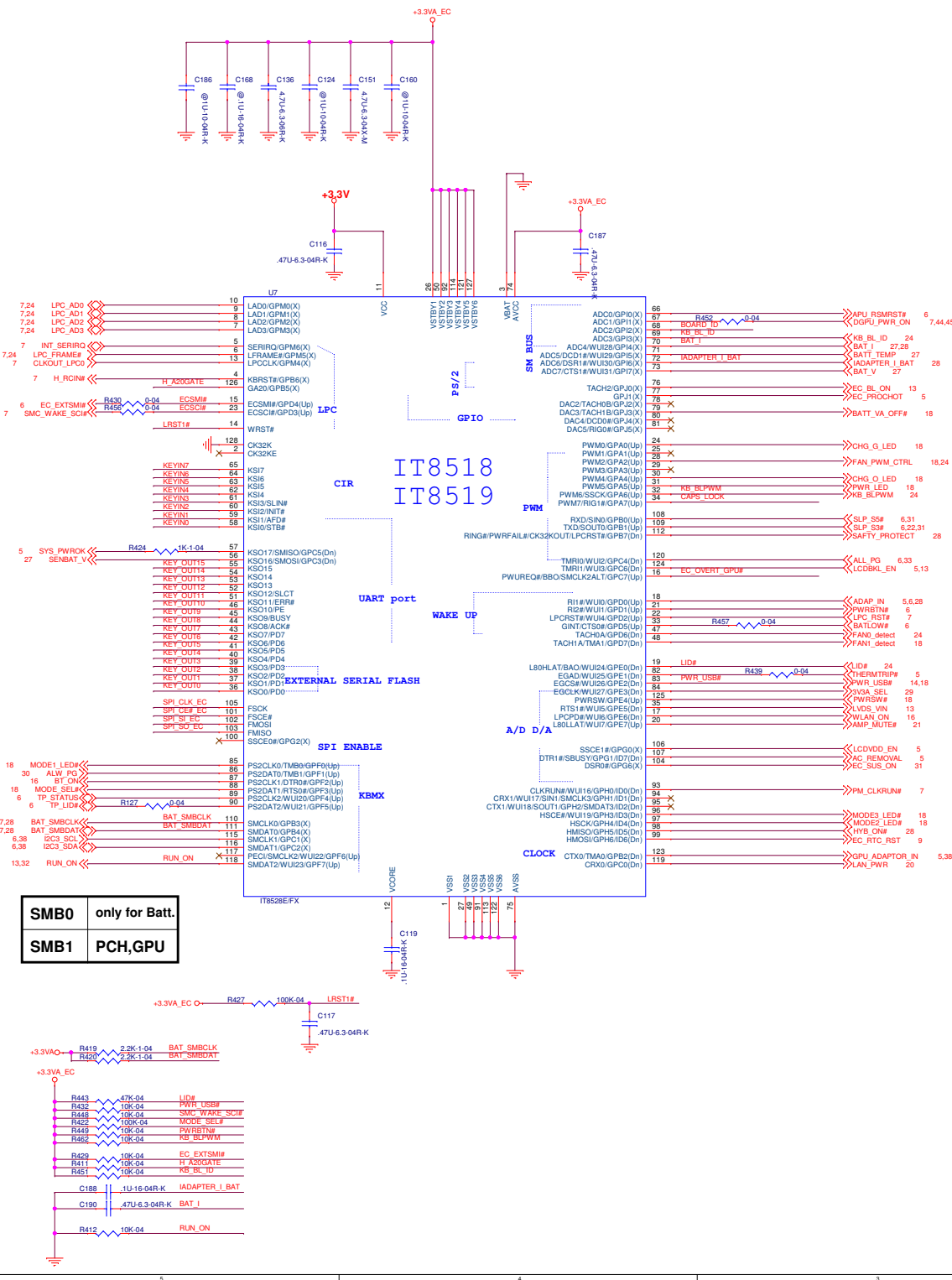
Audio&LAN DB CONN.



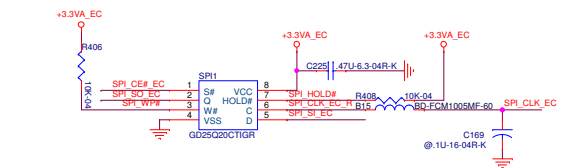




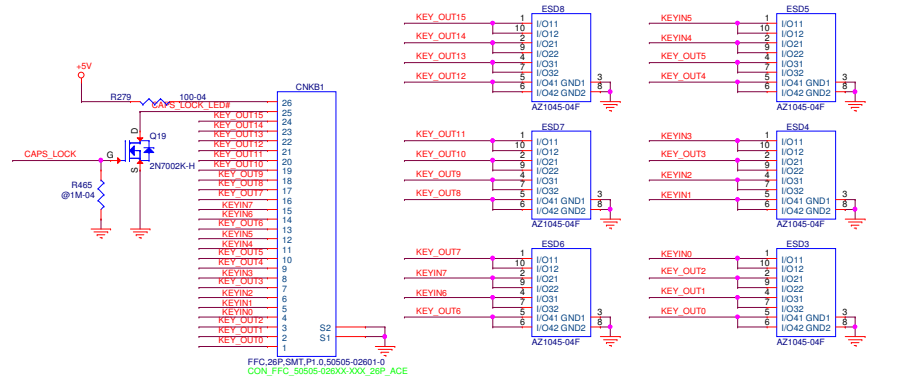
[illegible]



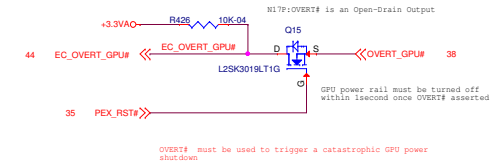
EC FLASH ROM(SPI)



KEYBOARD

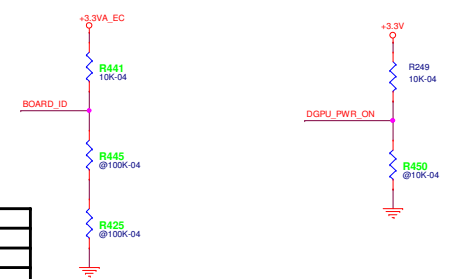


GPU Over Temperature Protection



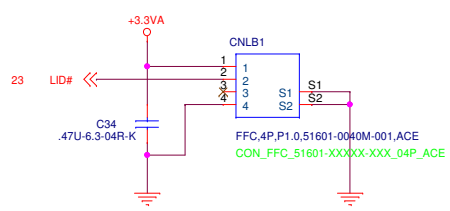
Platform ID

With MX150, install PH R & remove PD R
without MX150, install PD R & remove PH R

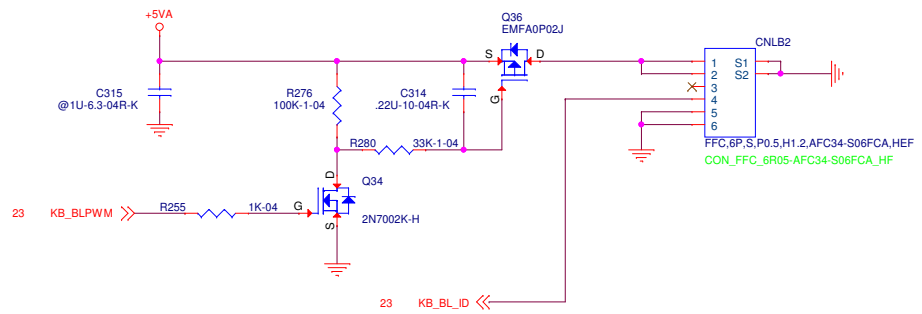


No.	Keyboard_ID	Description	R1	R2	MEMO
1	(3.3V)	PF4PN3F			
2	(2.8V)		56K-1-04	0-04	
3	(2.6V)		36K-1-04	1.24K-1-04	
4	(2.4V)		26.7K-1-04	0-04	
5			15.4K-1-04	0-04	
6	(2.0V)		12K-1-04	0-04	
7	(1.65V)				
8	(1.2V)		5.62K-1-04	100-1-04	
9	(0.8V)		3.24K-1-04	0-04	
10	(0.4V)		1.33K-1-04	75-1-04	
11	(0.0V)	PFSRN3G	0-04	0-04	

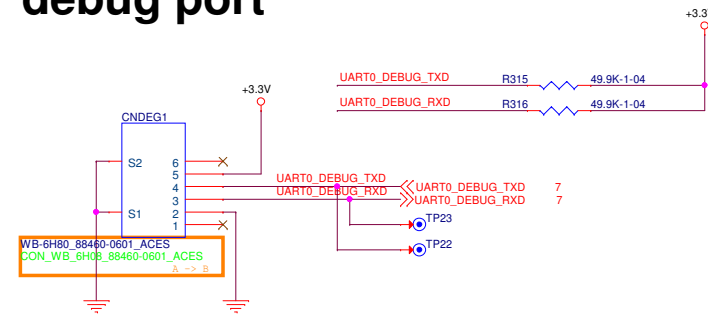
LID Switch CONN



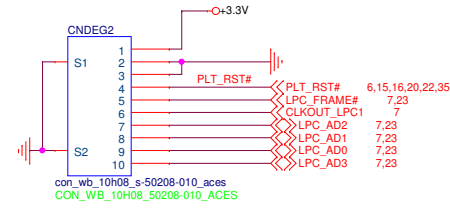
KB Back-Light CONN



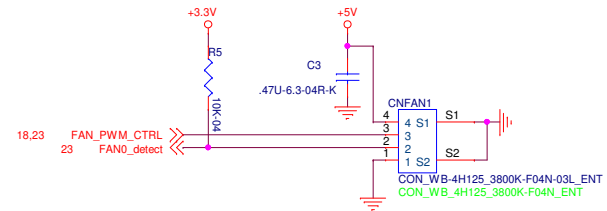
UART debug port



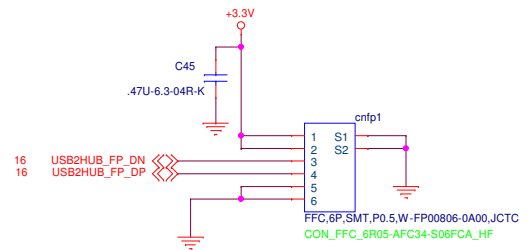
LPC debug port



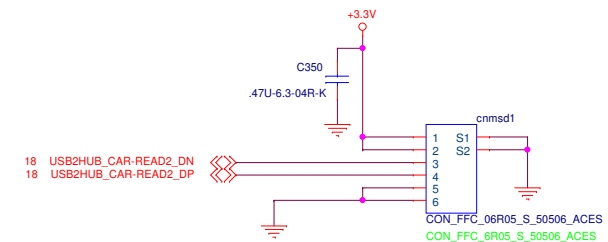
FAN CONTROLLER CONN

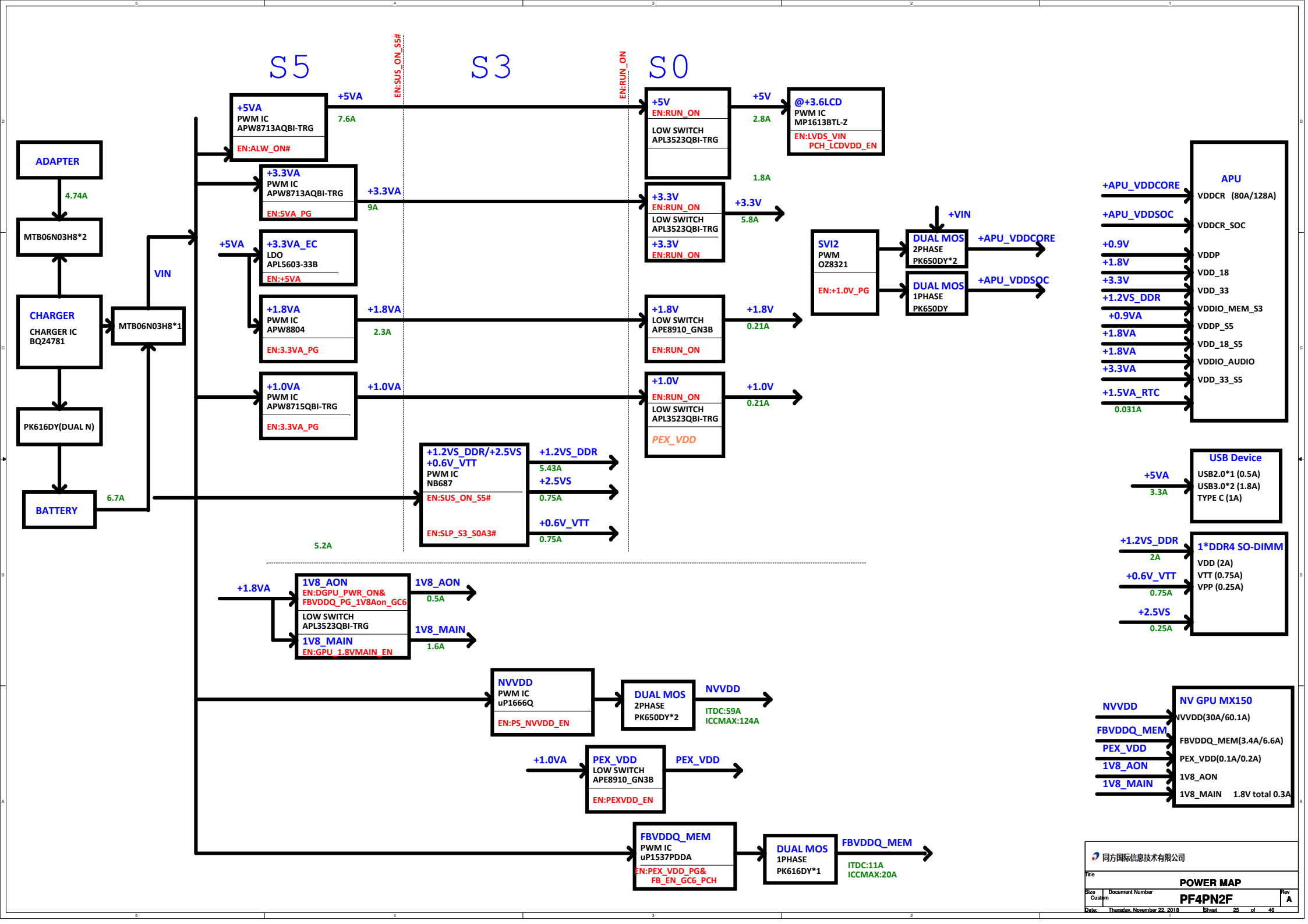


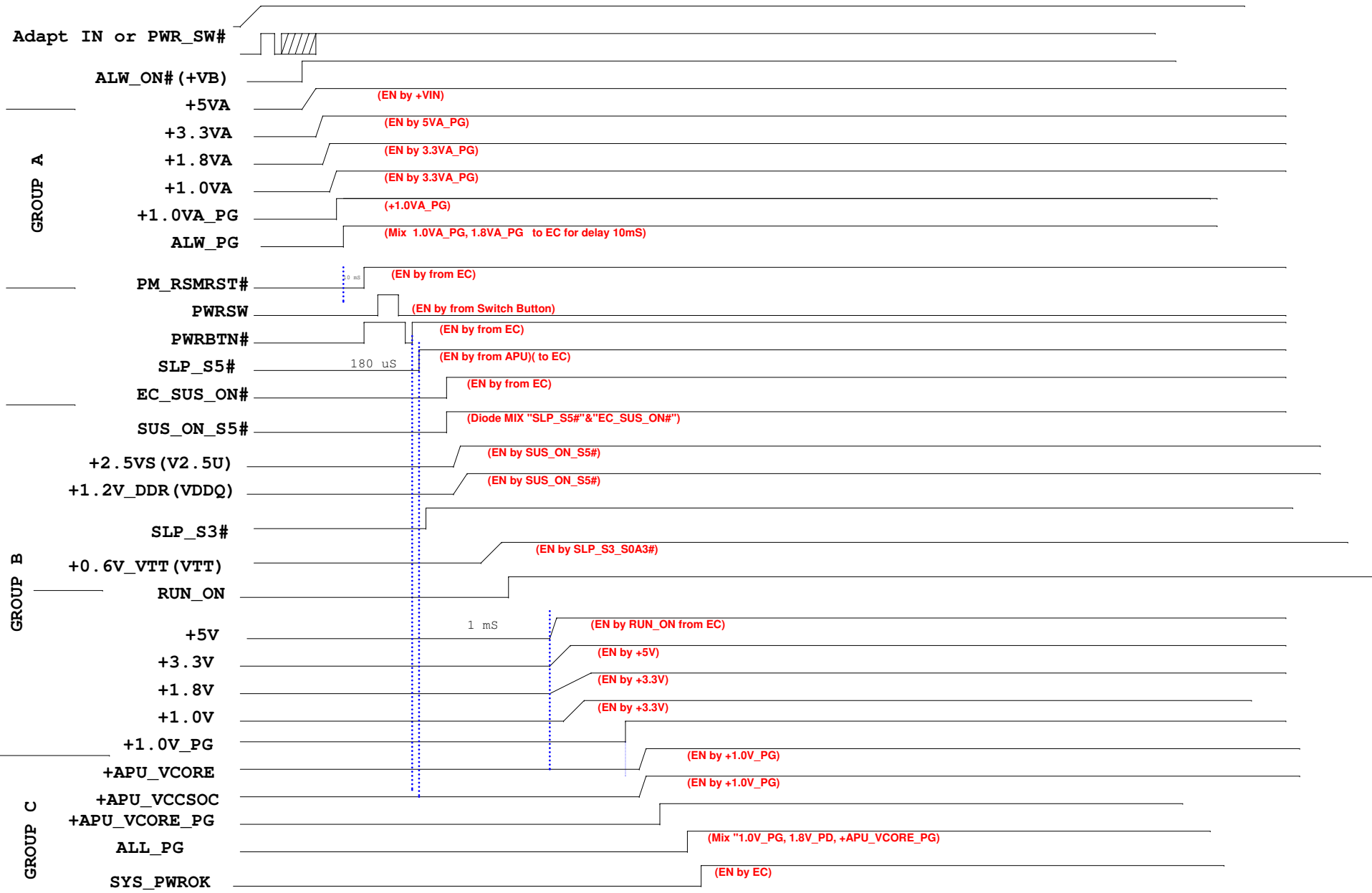
FINGER PRINTER CONN



Micro SD2 CONN



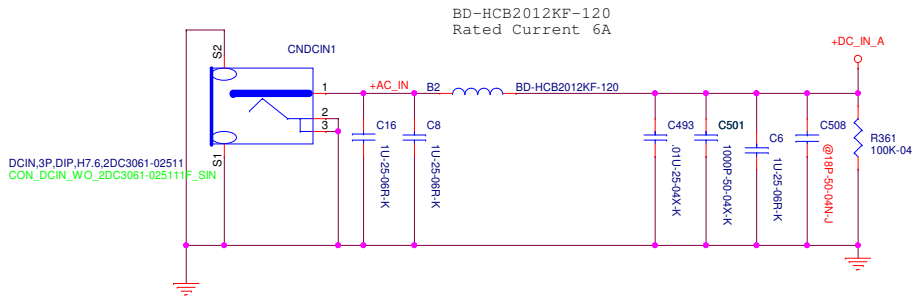




POWER ON SEQUENCE

+DC_IN

EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms



DCIN_3P_DIP_H7.6.2DC3061-02511
CON_DCIN_WO_2DC3061-02511F_SIN

BD-HCB2012KF-120
Rated Current 6A

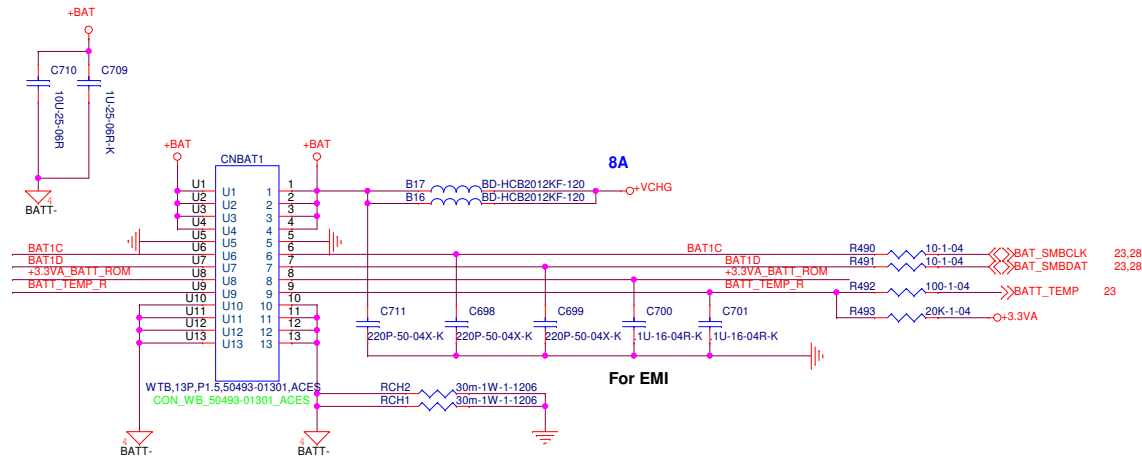
Battery Current Detect

RCH1 //RCH2 =7.5mohm

BAT_I	ICHG (0.0862V/1A)
2.0192V	4A
1.8468V	2A
1.7606V	1A
1.6744V	0A
1.5882V	-1A
1.5020V	-2A
1.3296V	-4A
1.1572V	-6A
0.9848V	-8A
0.8124V	-10A

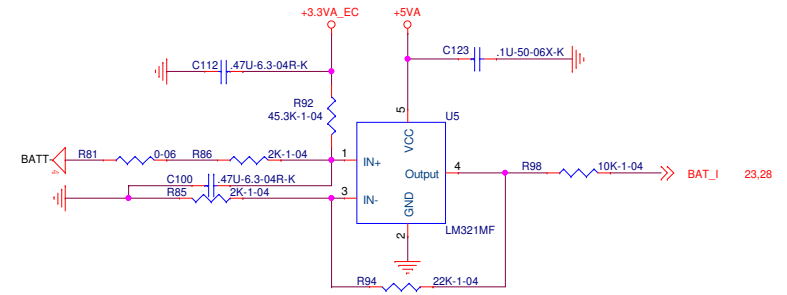
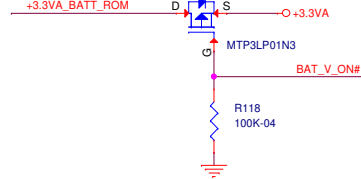
RCH1 //RCH2 =15mohm

BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A



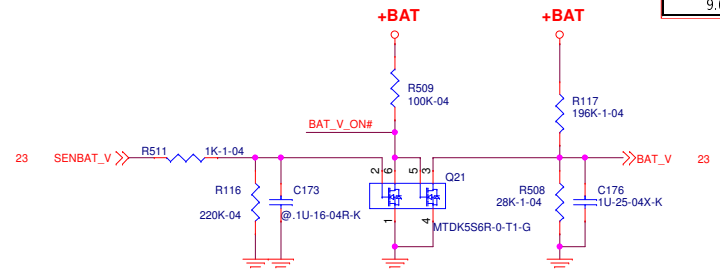
For EMI

Vgs_OFF= -0.4~-1.4



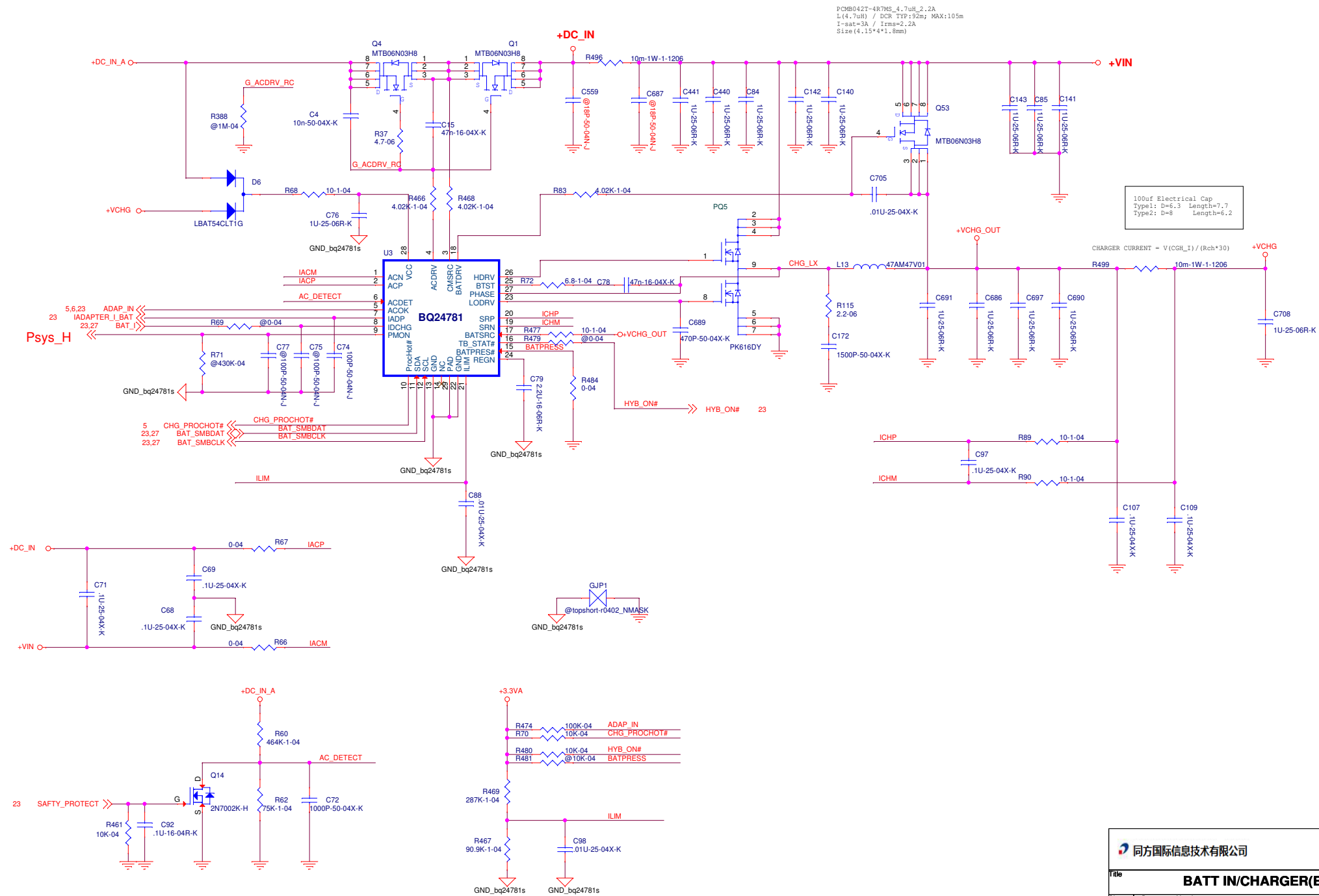
Battery Voltage Detect

BAT_Voltage	BAT_V
17.6V	2.2V
16.8V	2.1V
13.2V	1.65V
12.6V	1.575V
9.0V	1.125V



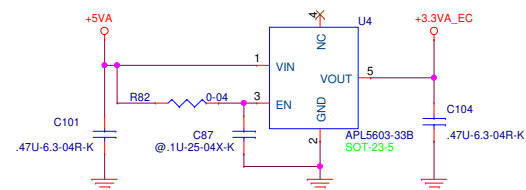
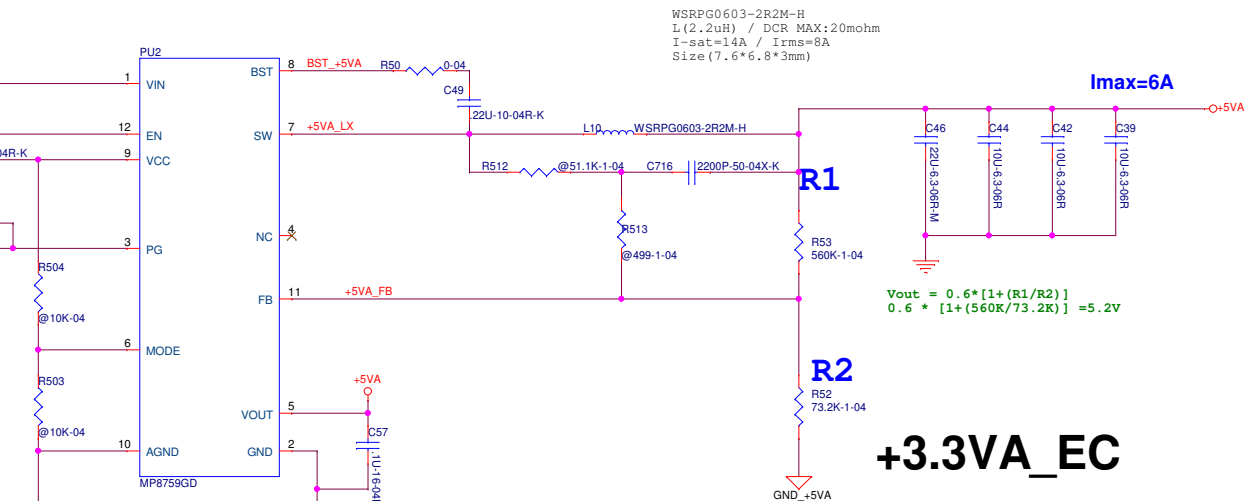
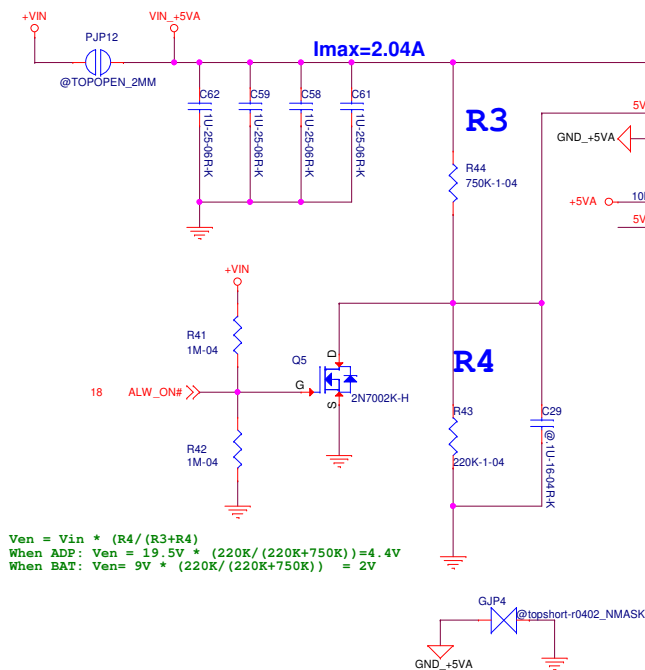
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DC IN/BAT_IN			
Size	Document Number	Rev	
Custom	PF4PN2F	A	
Date:	Thursday, November 22, 2018	Sheet	27 of 46

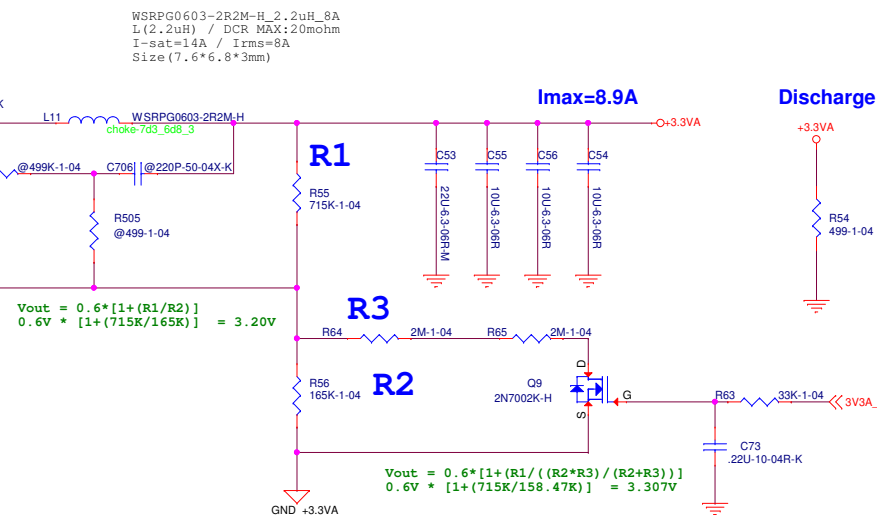
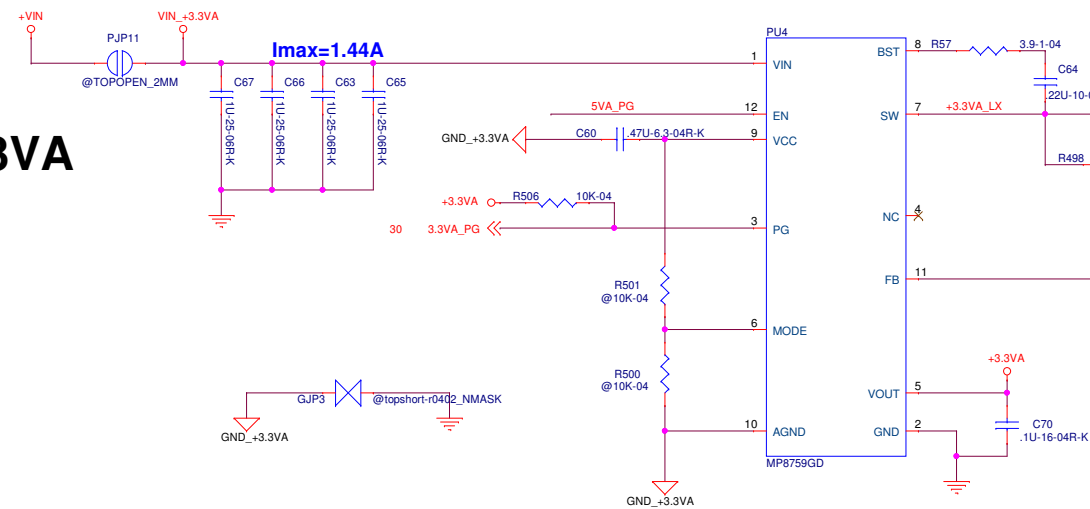


100uf Electrical Cap
Type1: D=6.3 Length=7.7
Type2: D=8 Length=6.2

+5VA



+3.3VA



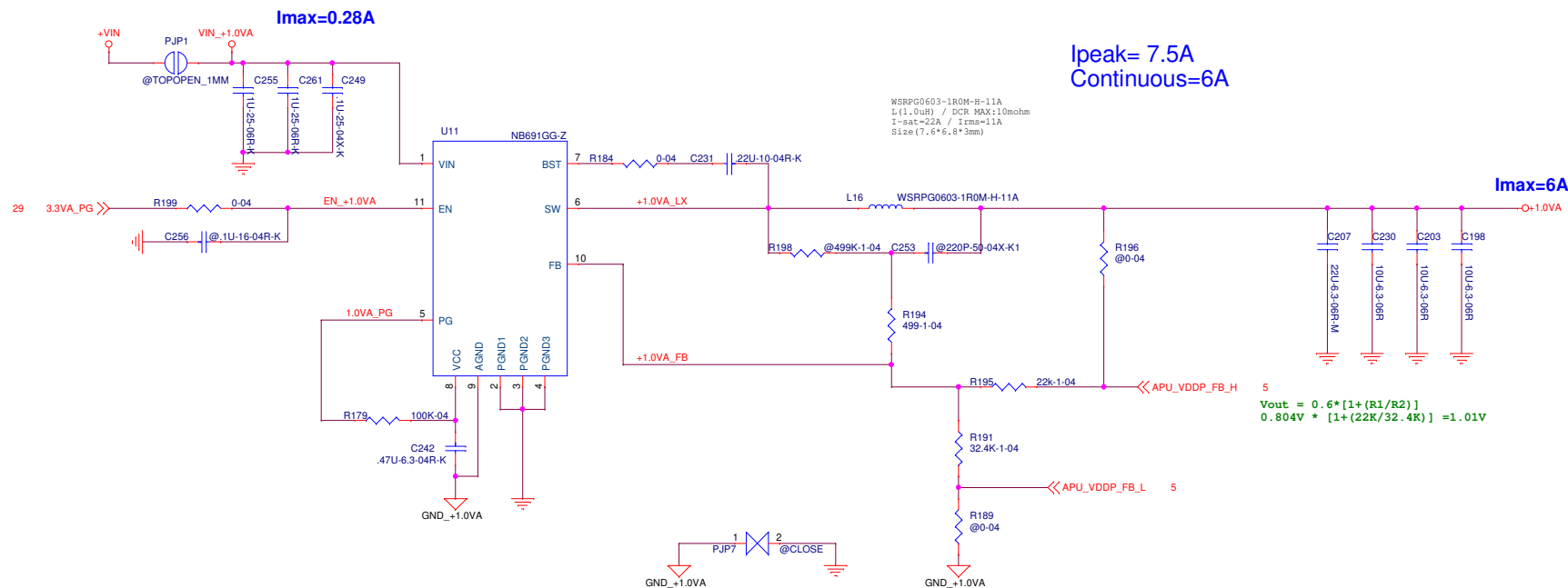
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Title **POWER +5VA/+3.3VA/+3.3VA EC**

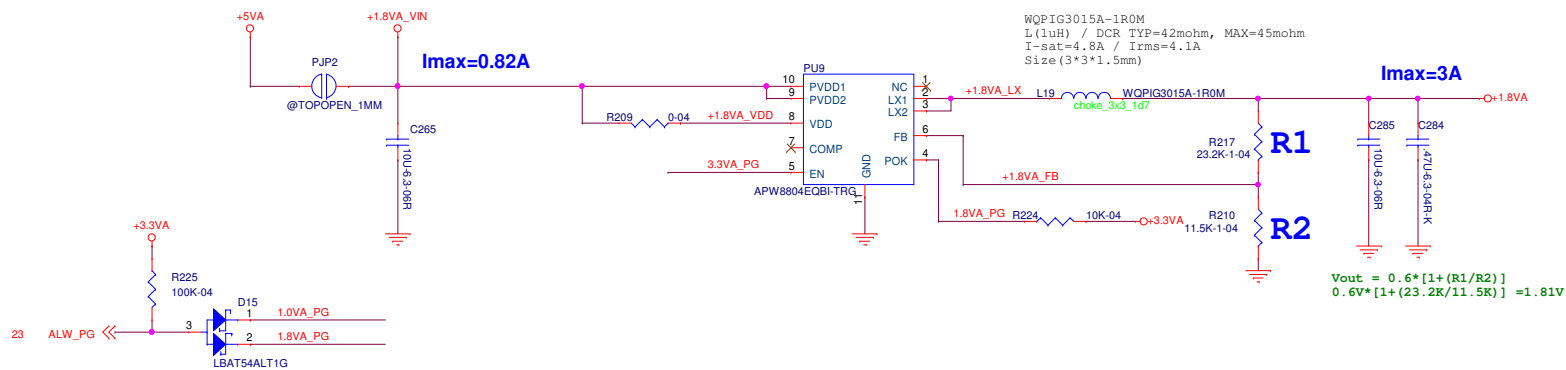
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+1.0VA



+1.8VA



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Title POWER_1.0VA/+1.8VA

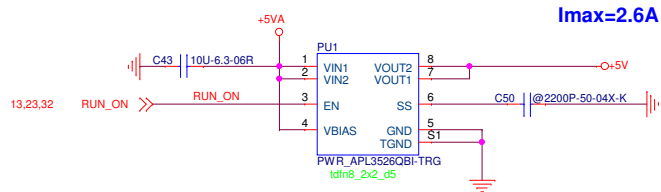
Size Custom Document Number PF4PN2F

Date: Thursday, November 22, 2018 Sheet 30 of 46

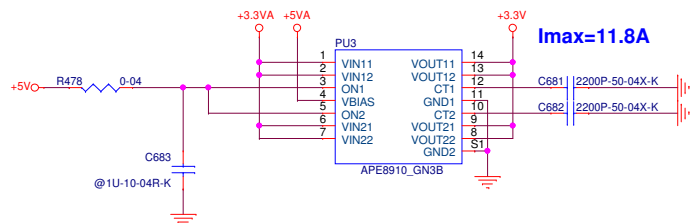
Rev A



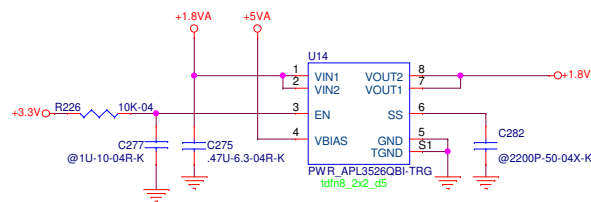
+5V



+3.3V

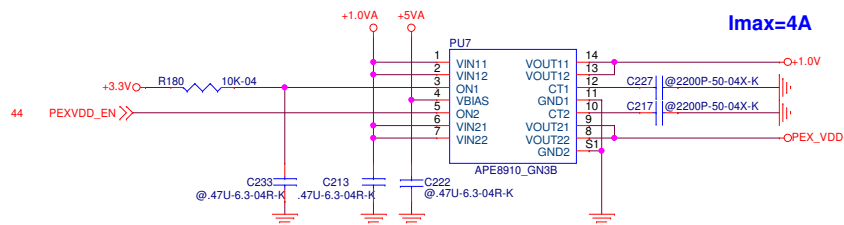


+1.8V

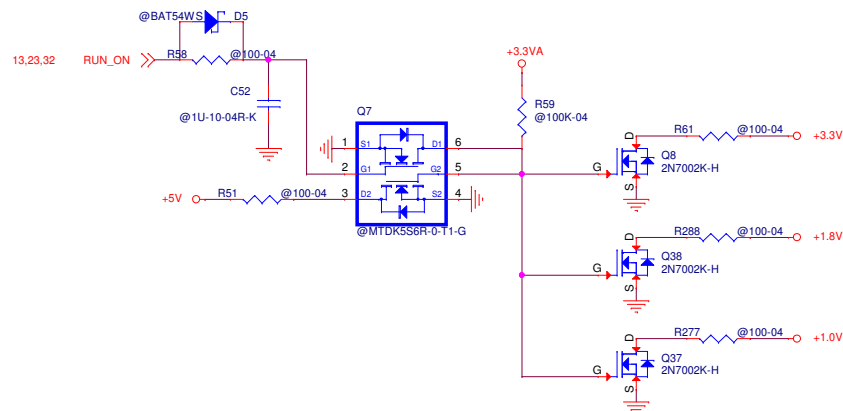


+1.0V

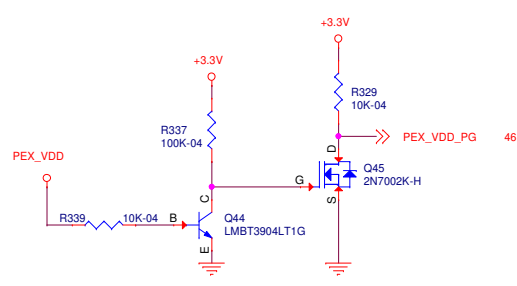
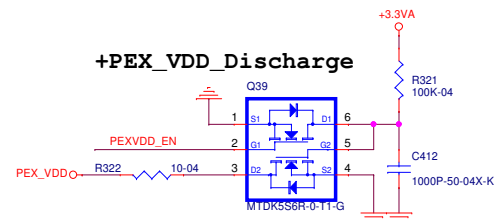
PEX_VDD



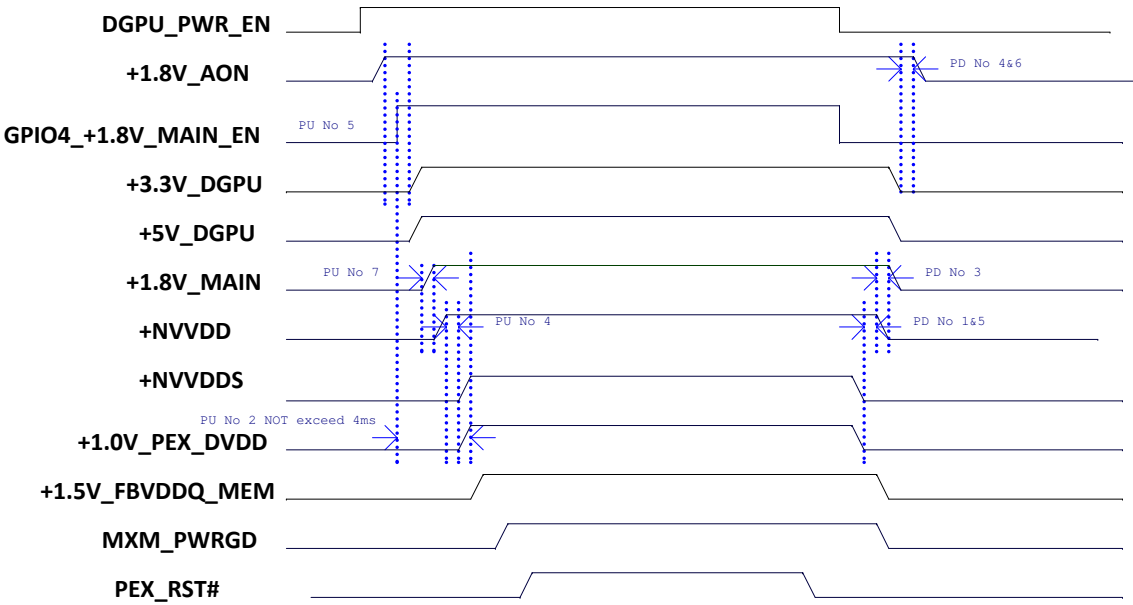
Discharge



+PEX_VDD_Discharge



DGPU POWER SEQUENCE

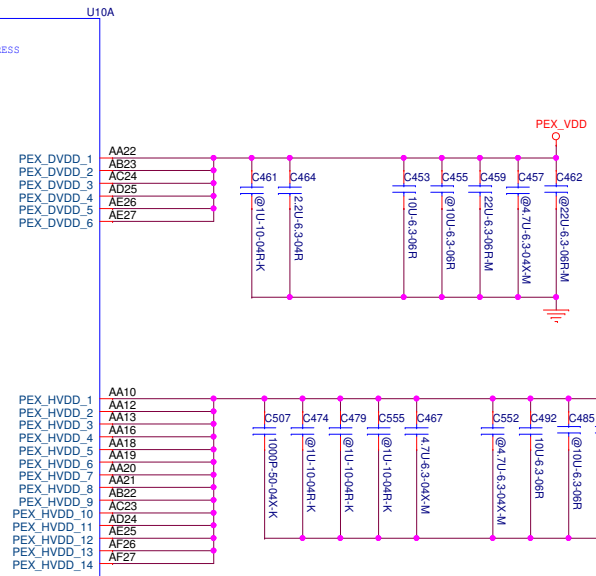
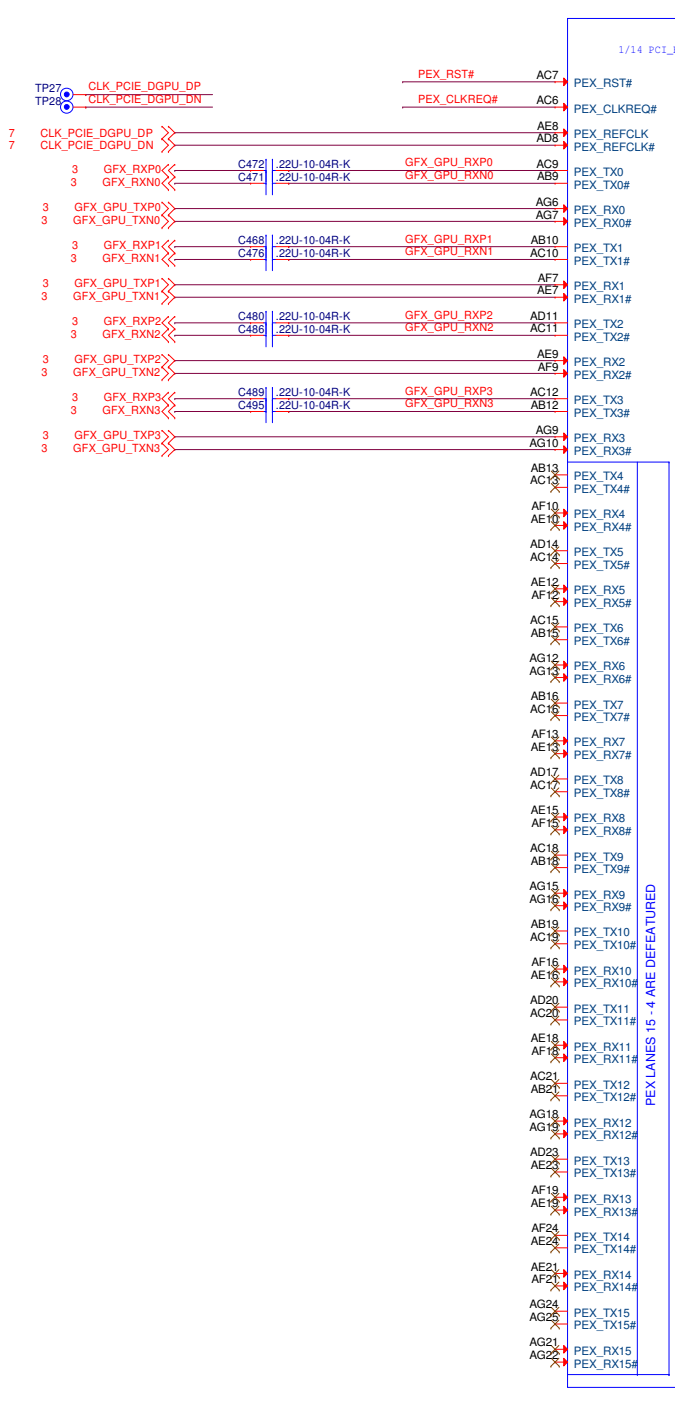


POWER UP sequence is required:+1.8V_AON->+1.8V_MAIN->+NVVDD->+NVVDDS/+1.0V_PEX_DVDD->+1.5V_FBVDDQ_MEM

- 1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
- 2.t1 From +1.8V_MAIN_EN to +1.0V_PEX_DVDD(+NVVDD_PG00D) must NOT exceed 4ms.
- 3.The ramp-up overshoot should not exceed the silicon reliability limit voltage
- 4.Power up +NVVDD must be 90% before +1.0V+PEX_DVDD and NVVDDS can start ramp up.
- 5.Power up +1.8V_AON must be 90% before 3.3V ramp up.
- 6.All 3.3V devices that connect to the GPU must be powered after +1.8V_AON ; GPU can't have any 3.3V leakage path before +1.8V_AON present.
- 7.The propagation delay between +1.8V_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.

POWER DOWN sequence is required

- 1.+NVVDDS/+1.0V_PEX_DVDD must ramp down before NVVDD.
- 2.All other power rails can ramp down together with NVVDD.
- 3.+1.8V_MAIN must power down after NVVDD power down
- 3.The propagation delay between +1.8VMAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
- 4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
- 5.Power down NVVDDS and +1.0V_PEX_DVDD must be less than 10% before NVVDD can start ramp down.
- 6.Power down 3.3V must be less than 10% before +1.8V_AON can start ramp down.

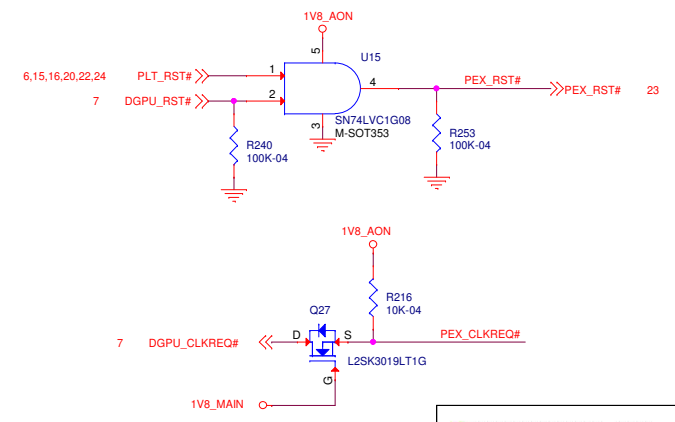
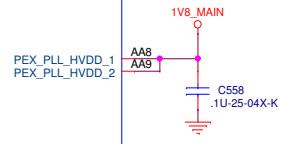


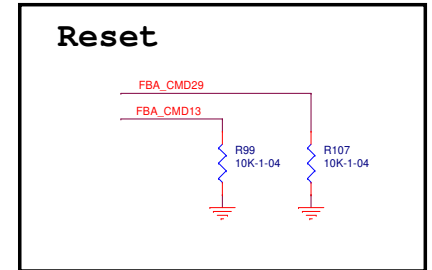
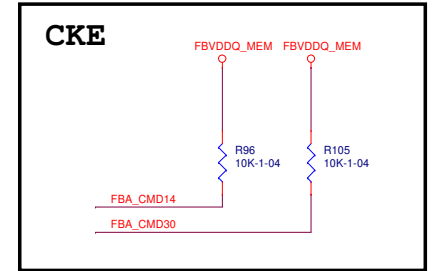
For N17S (GB2C-64) PIN-PEX_VDD

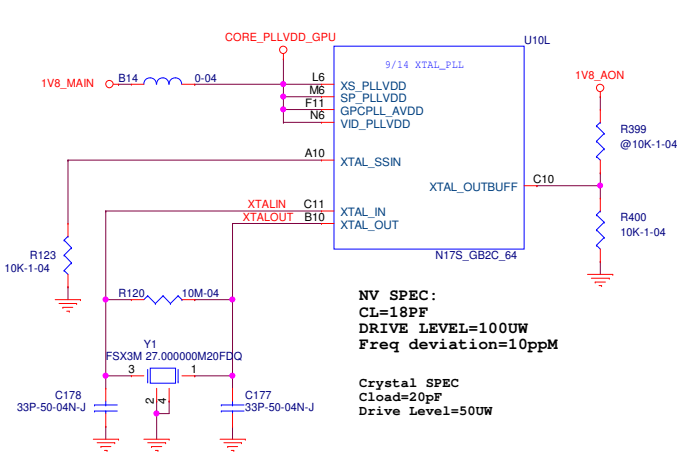
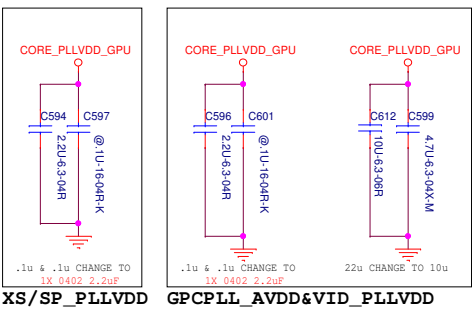
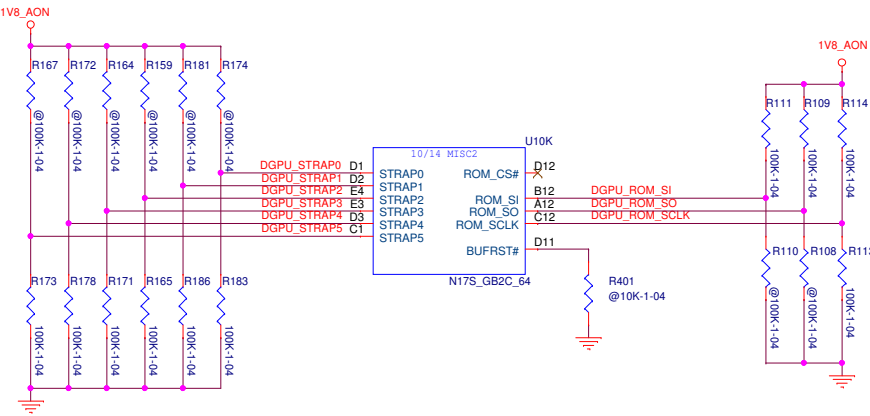
UNDER GPU	NEAR GPU	CHANGE TO	UNDER GPU	NEAR GPU
2x 0402 1uF	2x 0603 4.7uF 2x 0805 10uF 1x 0805 22uF		1x 0402 2.2uF	1x 0603 10uF 1x 0603 22uF

For N17S (GB2C-64) PIN-PEX_HVDD

UNDER GPU	NEAR GPU	CHANGE TO	UNDER GPU	NEAR GPU
4X 0402 1uF	2x 0603 4.7uF 2x 0805 10uF 1x 0805 22uF		1X 0402 4.7uF	1x 0603 10uF 1x 0603 22uF







GDDR5							
Density	Vendor	Part Number	Die	Strap	Strap2	Strap3	Strap0
2GB	Samsung	K4G81325FB-BC28	B-die	0X0	L	L	L
2GB	Micron	MT51J256M32HF-70:A	A-die	0X1	L	L	H
2GB	Hyunix	H5GC8H24MJR-ROC	M-die	0X2	L	H	L
1GB	Samsung	K4G41325FB-BC28	E-die	0X7	H	H	H
1GB	Hyunix	H5GC8H24MJR-ROC	A-die	0X6	H	H	L
1GB	Micron	EDW4032BAG-70-F	A-die	0X8	L	L	M

Voltage(V)			
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V 0.3V<pin voltage<0.5V		

Strap5,4,3 LLL

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE(Select)

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL(Select)

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER(Select)

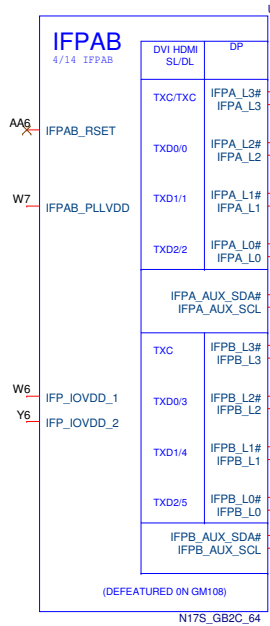
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE(Select)

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)			See This Row of Table 5.5
	Total Enabled for Audio (HDMI, DP or DVI)		
		Is IFPD used? (Only supports eDP.)	
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			

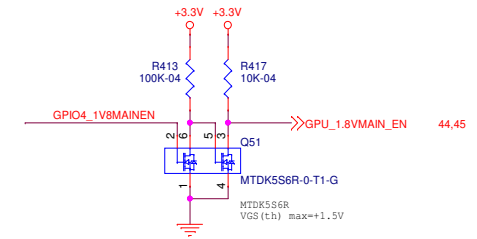
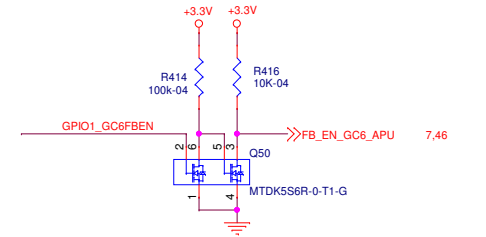
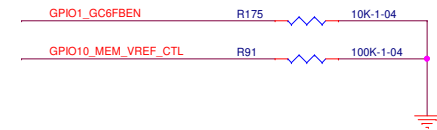
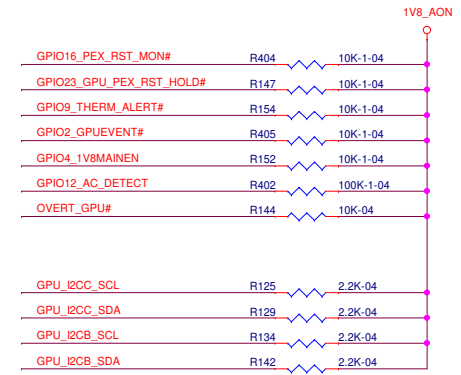
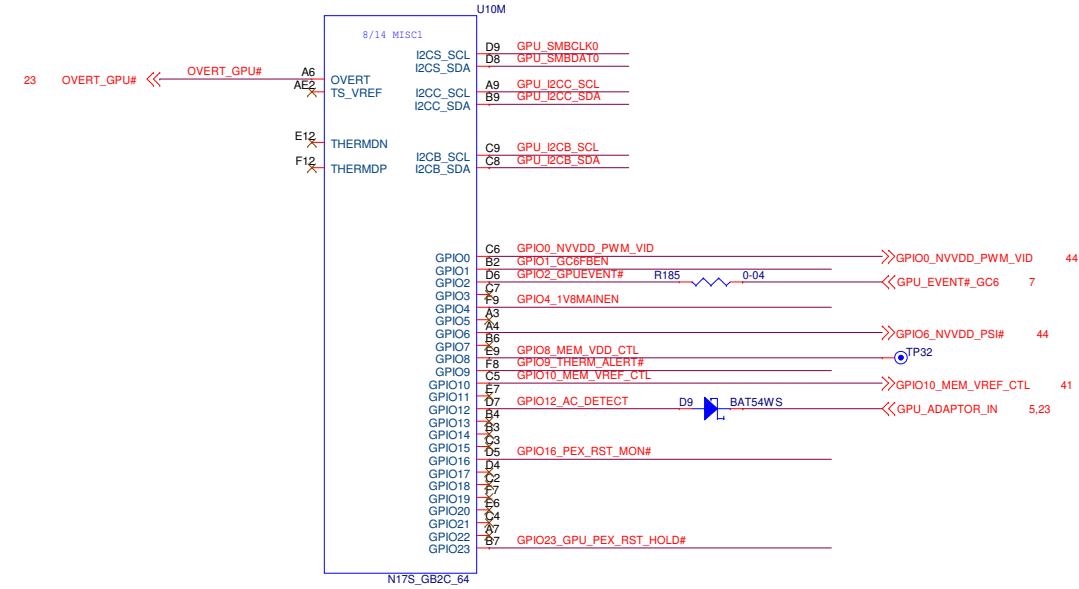
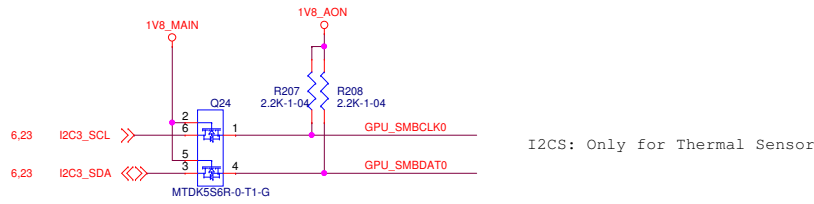


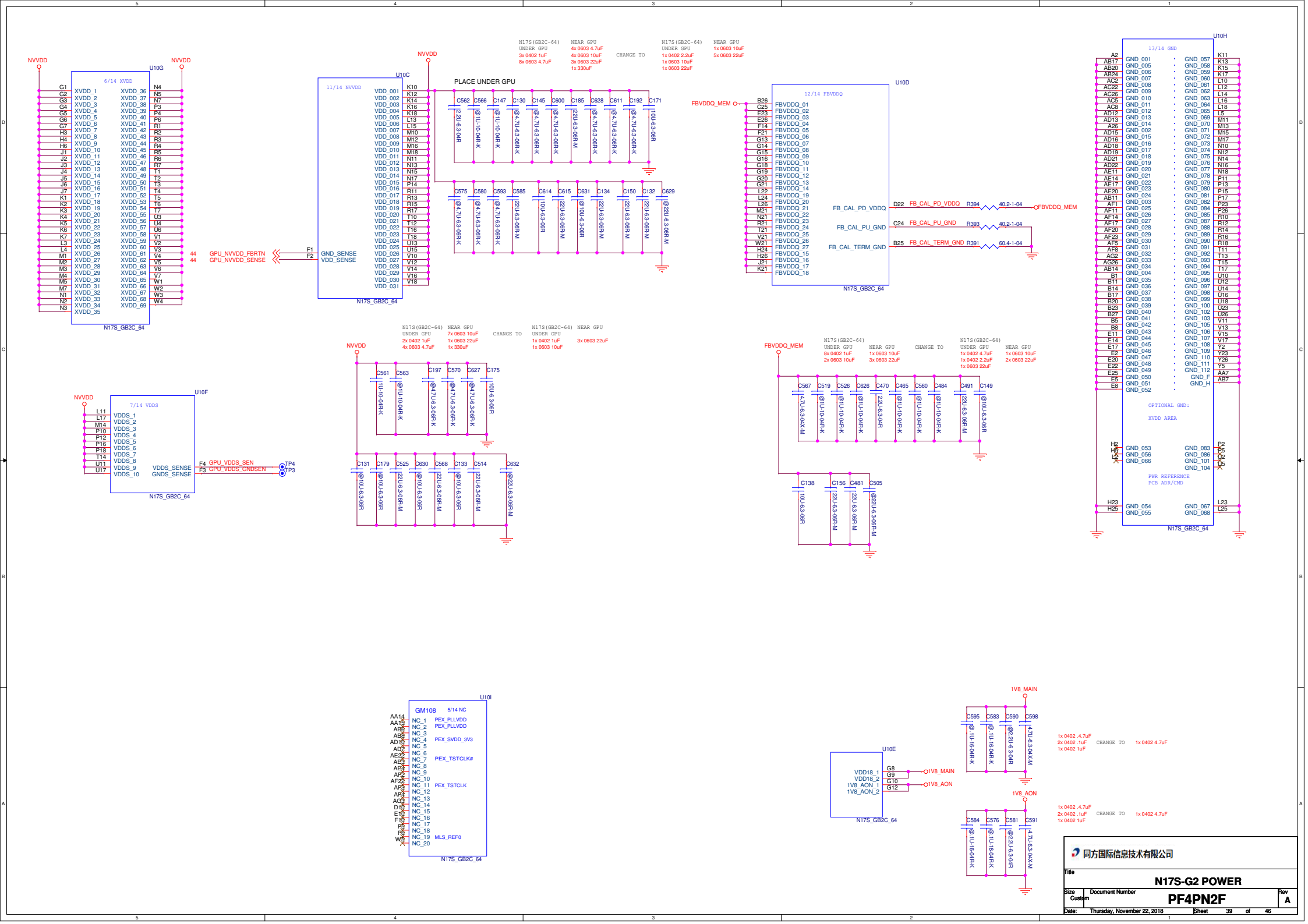
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Title N17S-G2 XTAL/IFP[A:F]

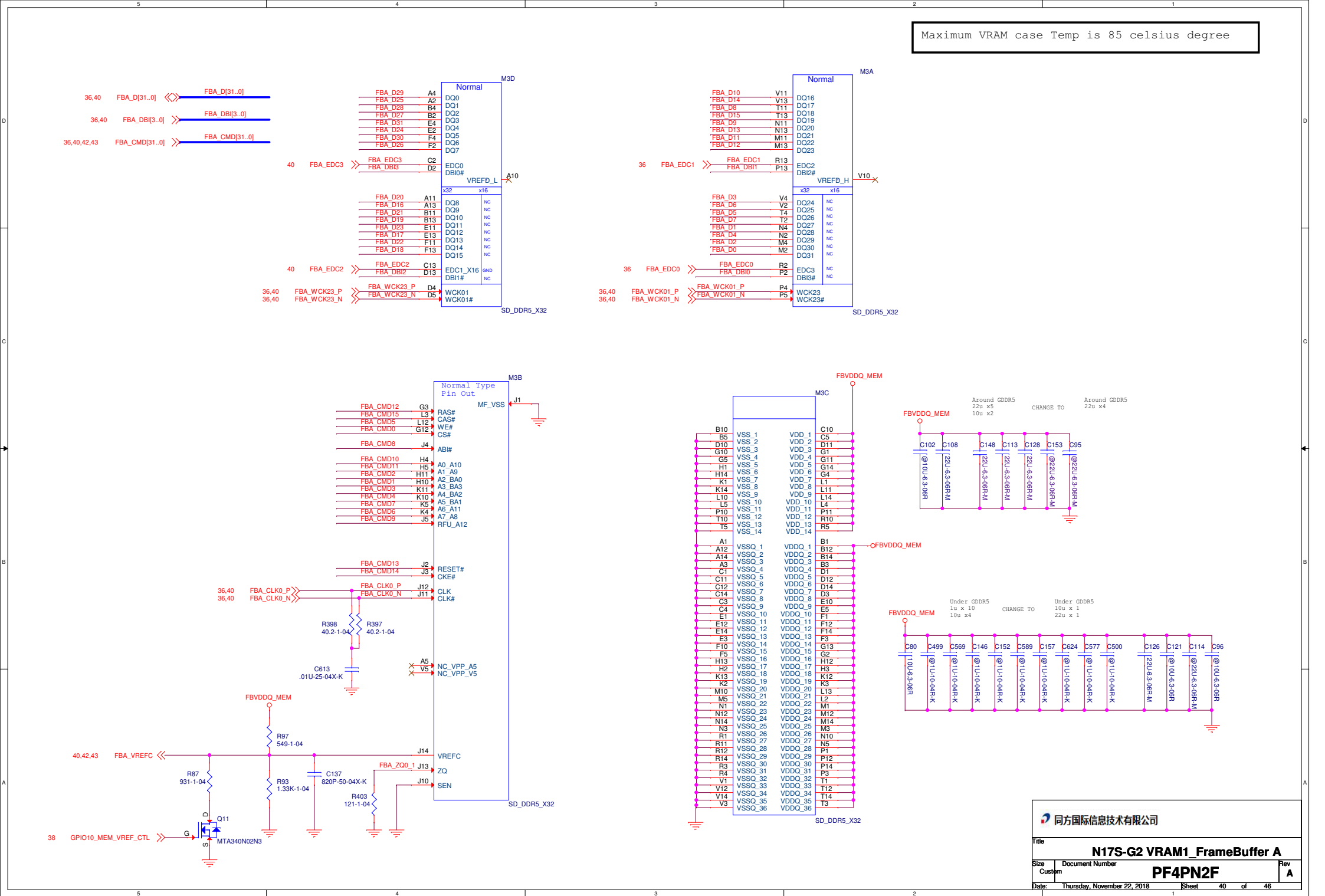
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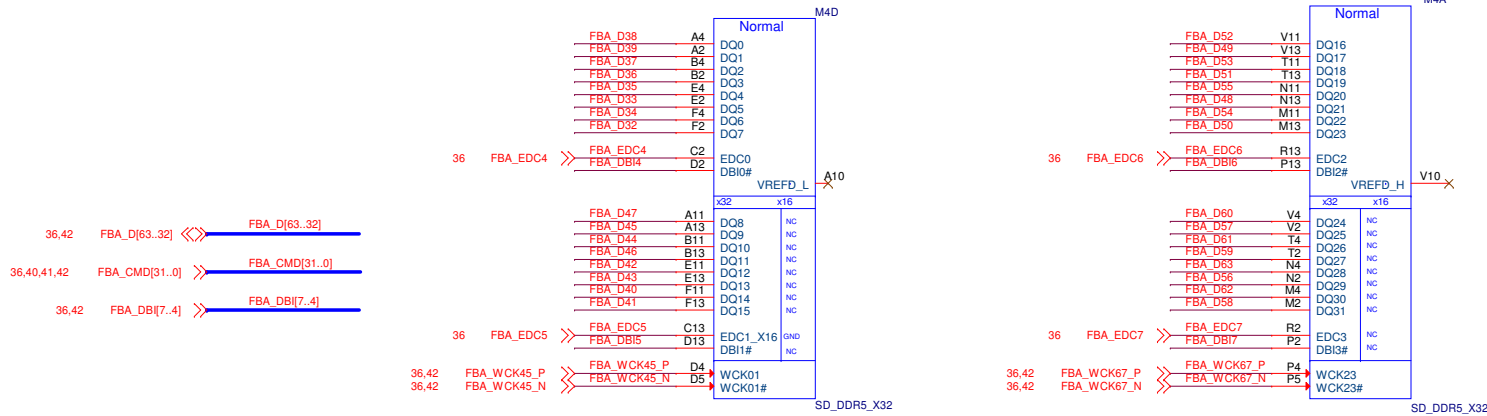




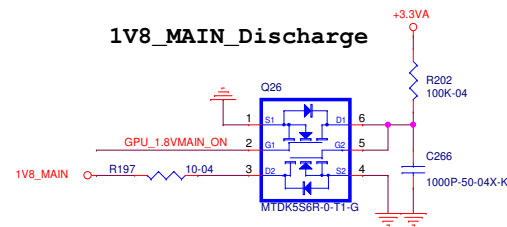
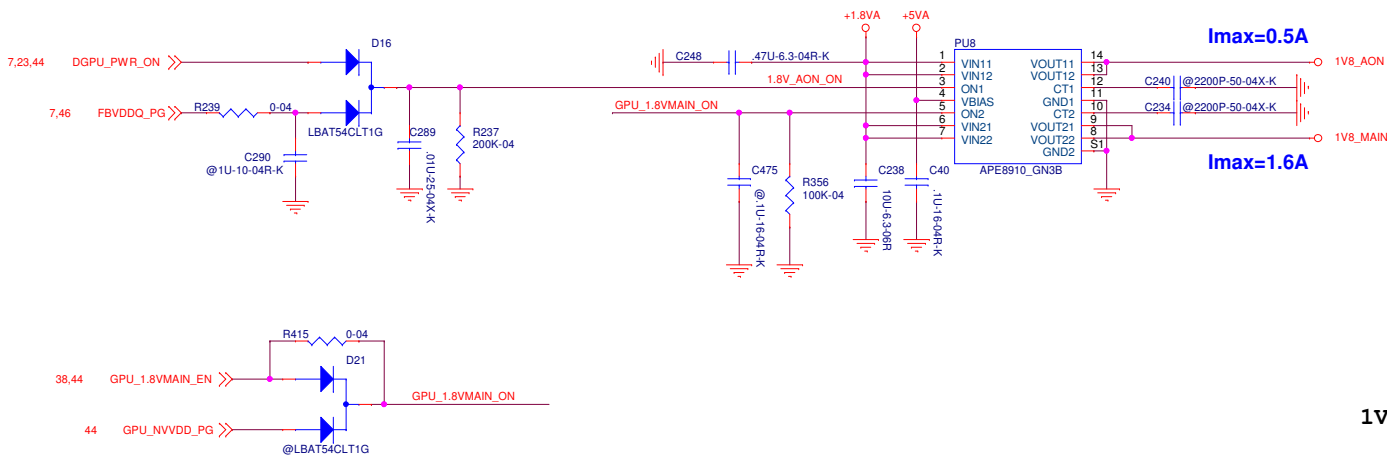
Maximum VRAM case Temp is 85 celsius degree



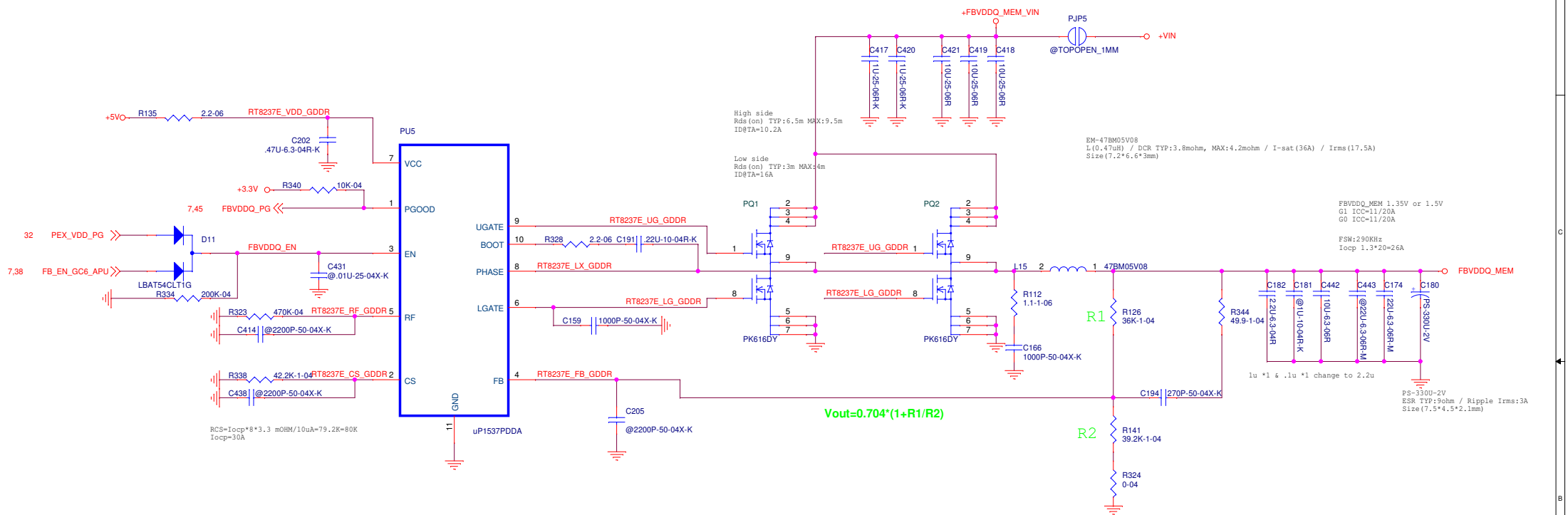
Maximum VRAM case Temp is 85 celcisus degree



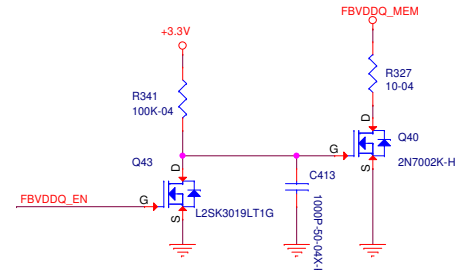
+1.8V_AON/+1.8V_MAIN

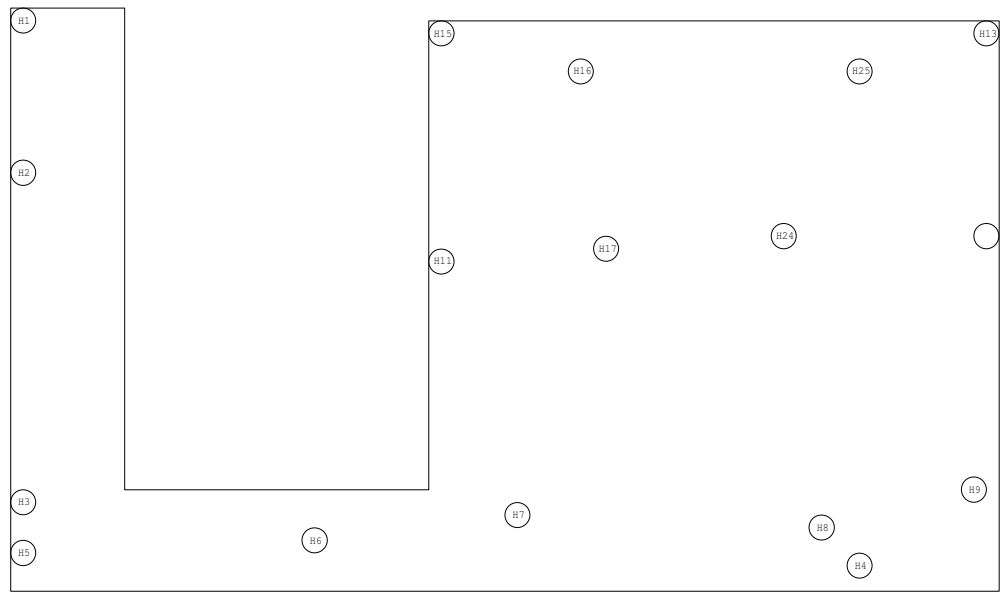


FBVDDQ_MEM

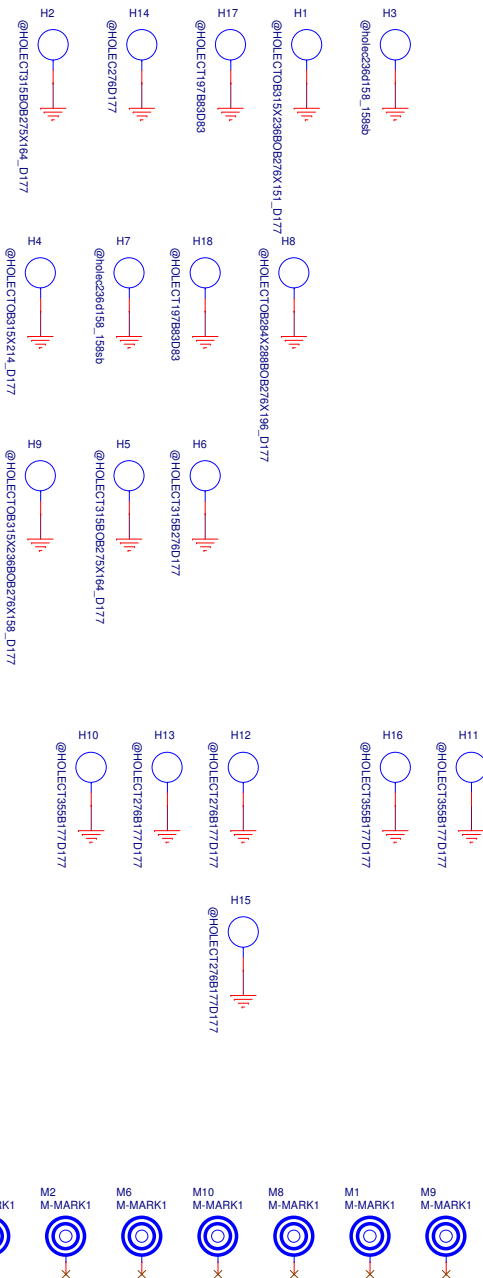


FBVDDQ_MEM_Discharge

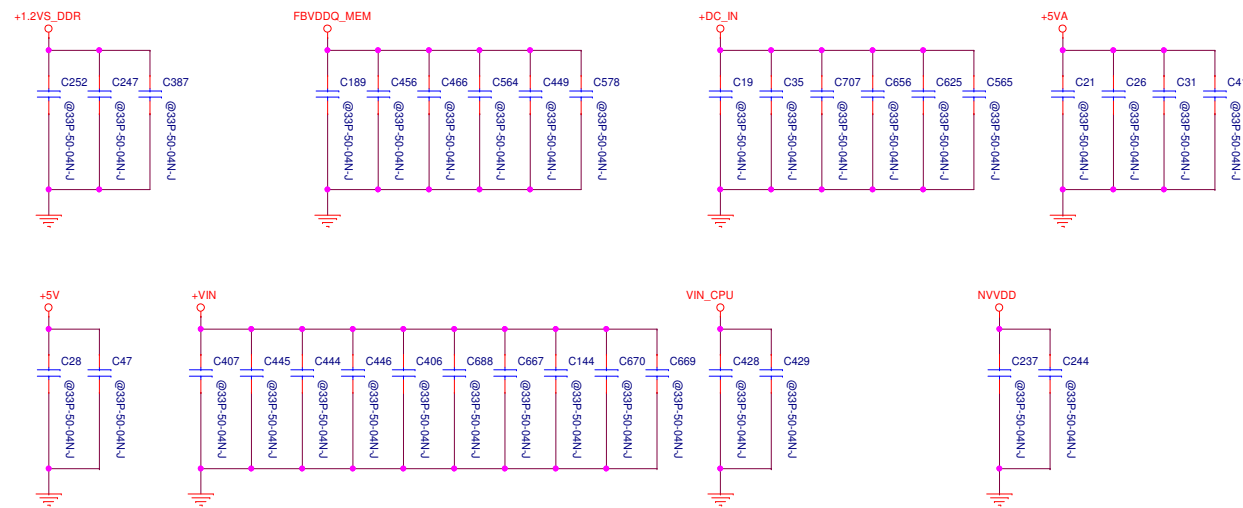




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